

NOTES: (UNLESS OTHERWISE SPECIFIED)

CHNG. CODE	SYM NO	REVISIONS		APPROVED	DATE
		DESCRIPTION			
-	A 8231	PRODUCTION RELEASE PER EN 82191		W.Brown	7/17/74
-	B 82682	REVISED SHTS 2,3,4,5 PER EN 82311		W.Brown	7/17/74
-	C 82682	REVISED SHTS 5 & 7 PER EN 82682		W.Brown	7/17/74

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
J2	J1
C21	
P1	

REFERENCE DRAWINGS	
95W0998	WIRE LIST
44P0684	BOARD ASSY P/L
44D0684	BOARD ASSY
40D0175	BOARD DETAIL

DR		varian data machines / a varian subsidiary	
CHK W.Brown	7/6/73	2722 michelson drive / irvine / california / 92664	
DSGN		TITLE	
ENGR W.Brown	7/6/73	LOGIC DIAGRAM	
APPD E.Hallinan	7/6/73	CARD READER CONTROLLER	
APPD		MODEL G20-2B	
THIS DOCUMENT MAY CONTAIN PROPRIETARY INFORMATION AND SUCH INFORMATION MAY NOT BE DISCLOSED TO OTHERS FOR ANY PURPOSE OR USED TO PRODUCE THE ARTICLE OR SUBJECT, WITHOUT WRITTEN PERMISSION FROM VDM			
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0455	C
SCALE		SHEET / OF 8	

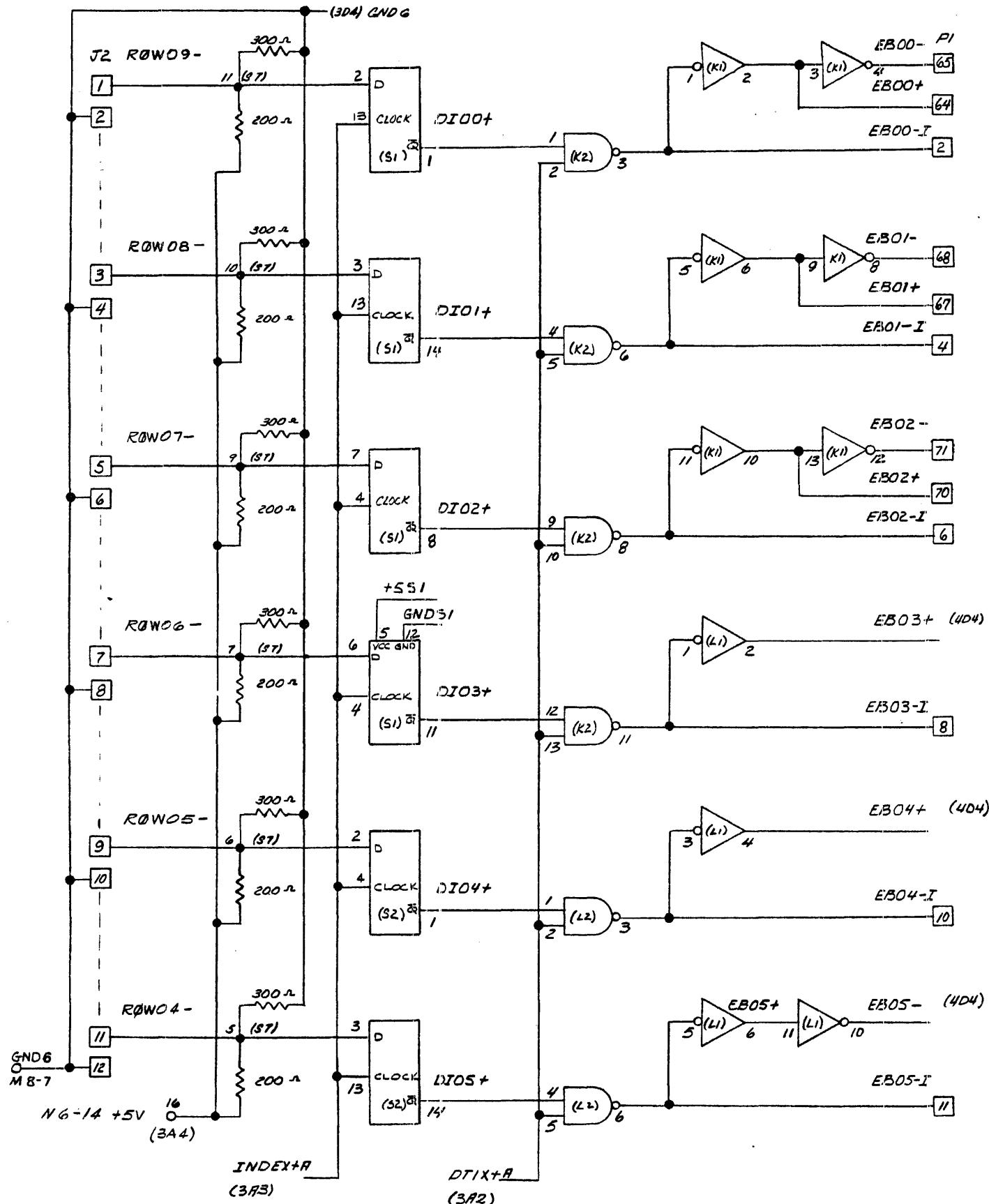
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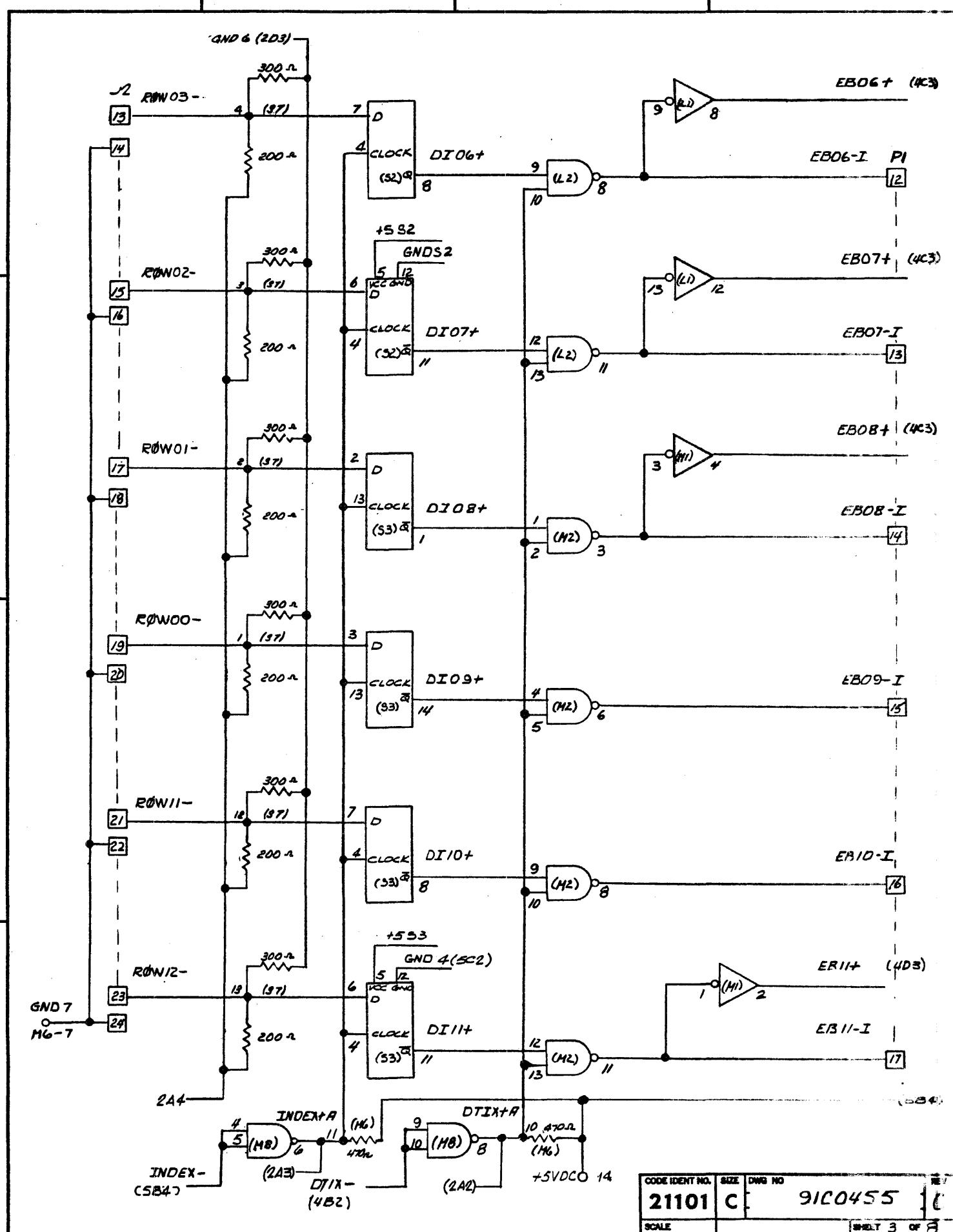
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D



A

CODE IDENT NO.	SIZE	DWG NO	REV
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SCALE		SHEET 2 OF 8	

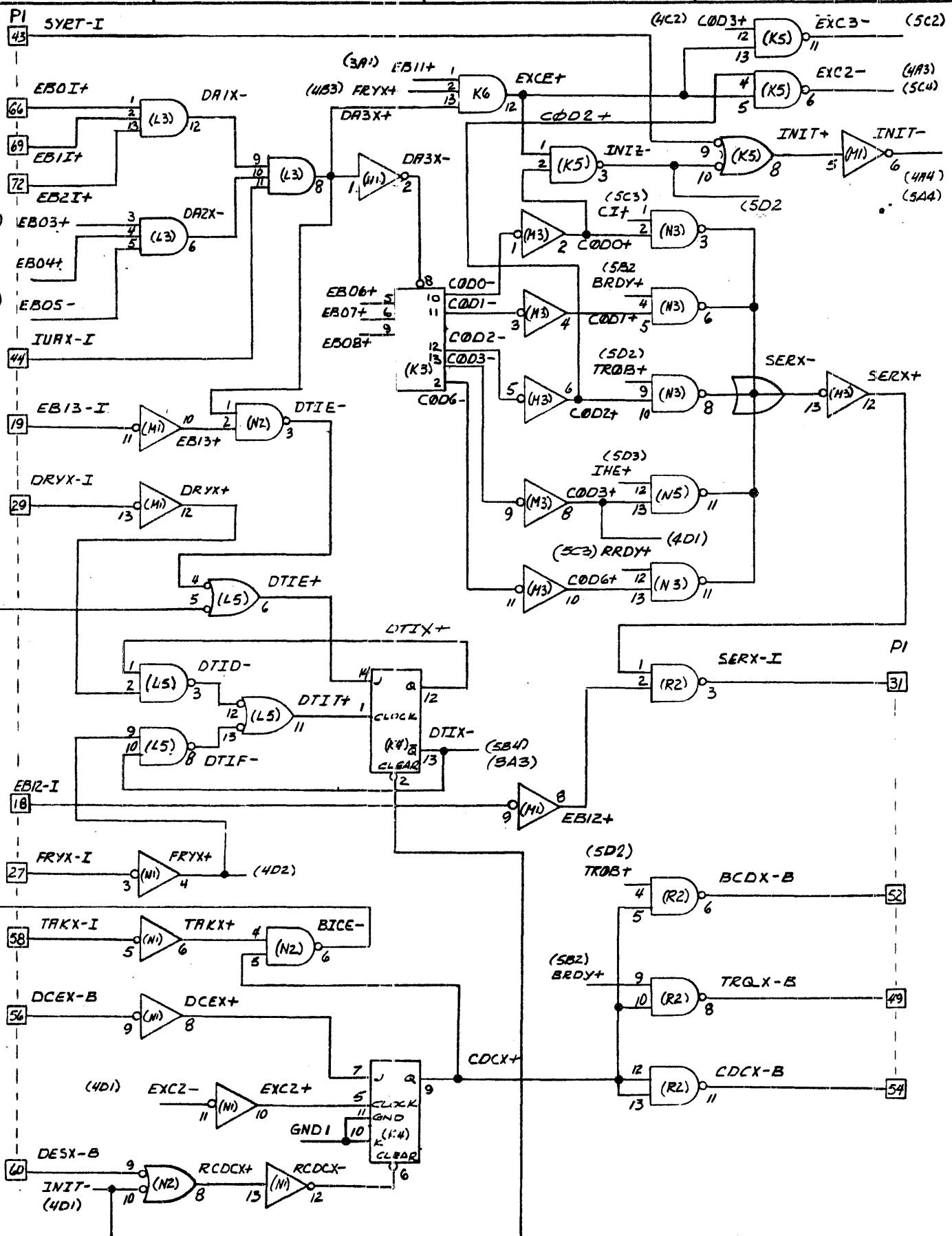


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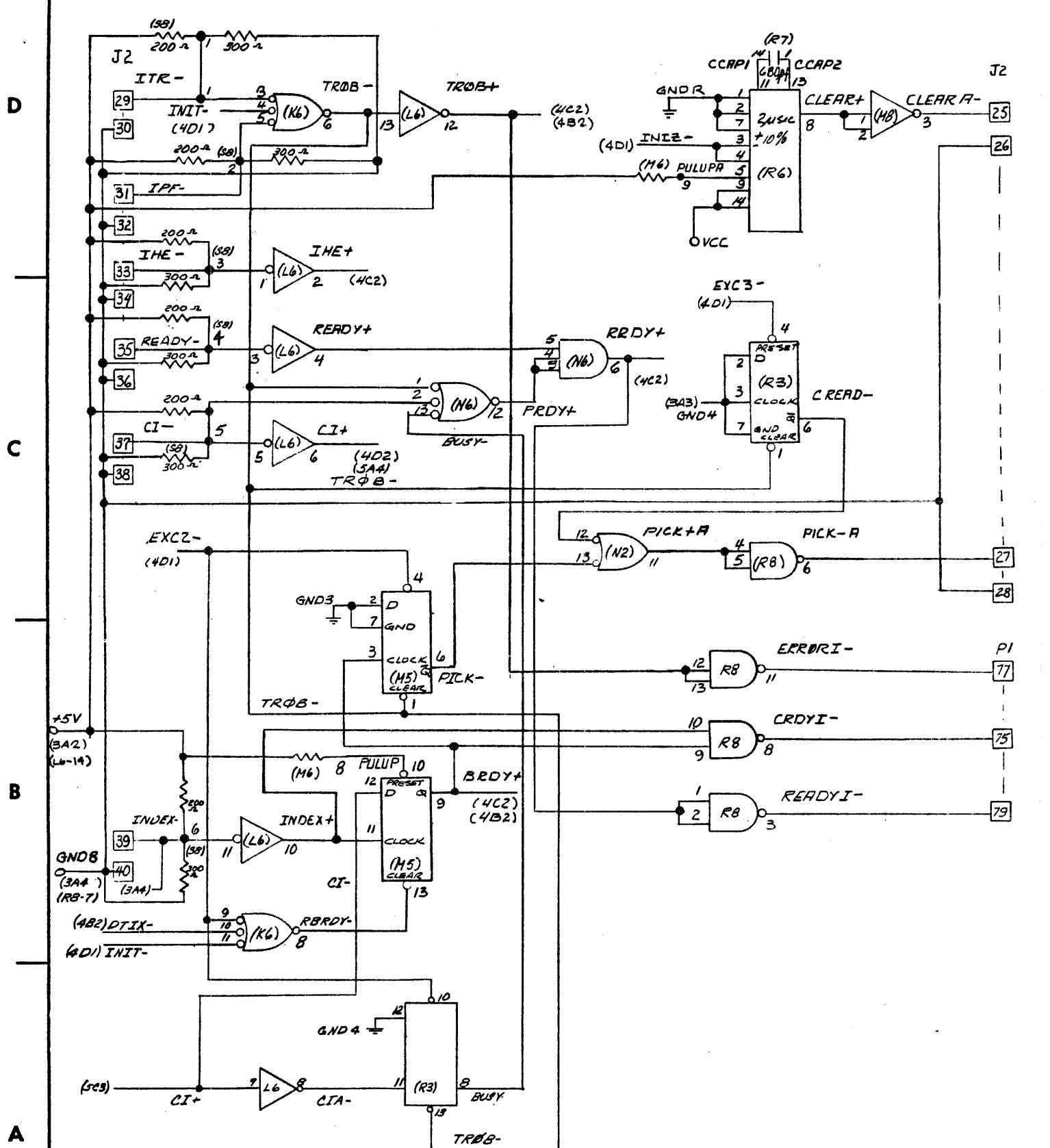


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NOTE UNLESS OTHERWISE SPECIFIED ALL RESISTORS
ARE 470 OHMS

CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91C0455	C
SCALE		SHEET 5 OF 2	

4

3

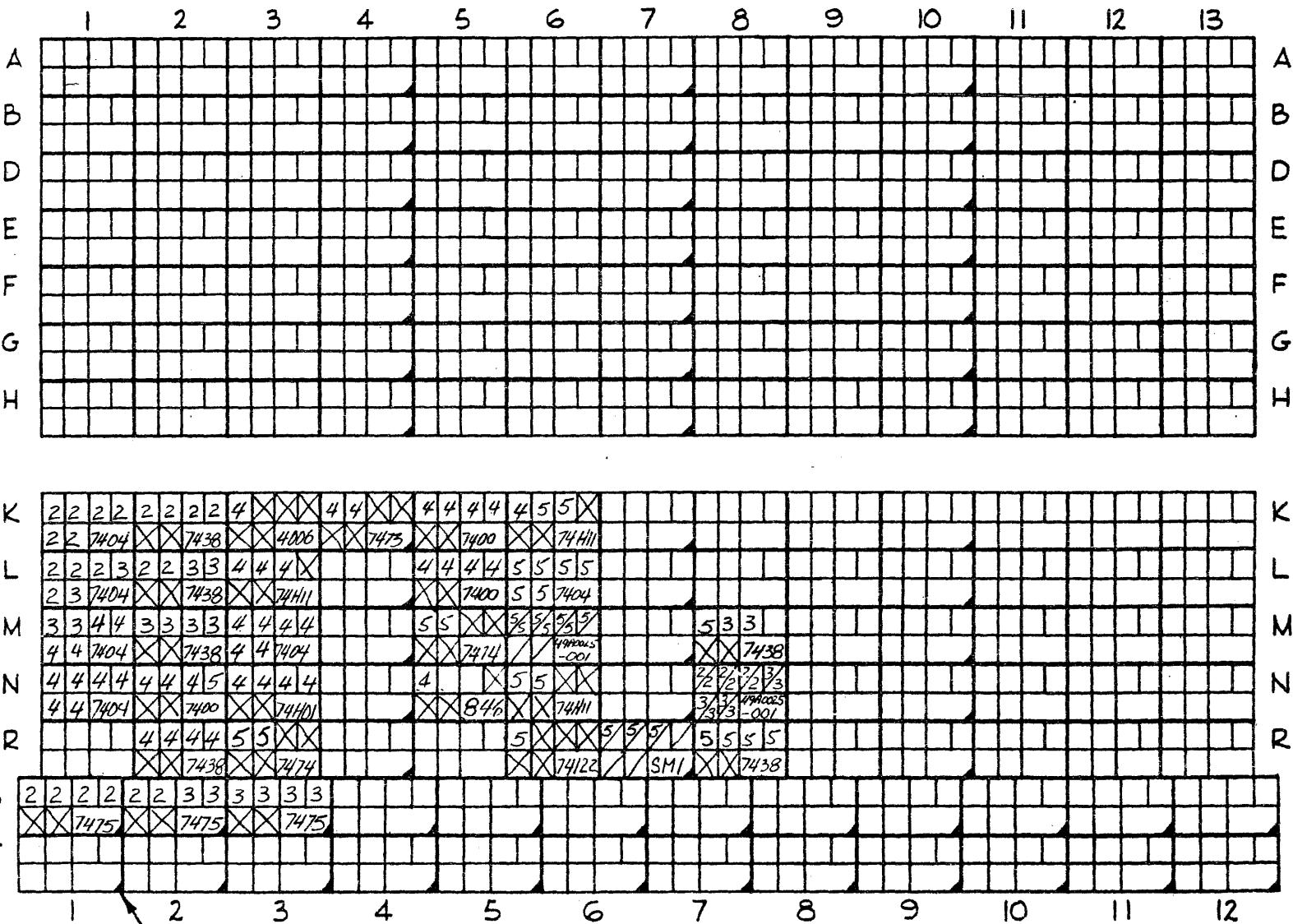
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1

	PI	PI	PI	J2
D	1	40	E82I+	R0W03- (304)
	2 E800-I (2D1)	41		13 GND 7 (304)
	3 GND	42		14 R0W02- (3C4)
	4 E801-I (2C1)	43 SYRT-I (404)	75 CRDYI- (5B1)	15 GND 7 (3C4)
	5 GND	44 IUAX-I (4A4)	76	16 R0W01- (3C4)
	6 E802-I (2C1)	45	77 ERRORI- (5B1)	17 GND 7 (3C4)
	7 GND	46	78 READYI- (5B1)	18 R0W00- (3B4)
	8 E803-I (2B1)	47	79	19 GND 7 (3B4)
	9 GND	48 GND	80	20 R0W11- (3B4)
C	10 E804-I (2B1)	49 TRQX-B (4A1)	114	21 GND 7 (3B4)
	11 E805-I (2A1)	50	115	22 R0W12- (3A4)
	12 E806-I (3D1)	51	116	23 GND 7 3A2
	13 E807-I (3C1)	52 BCDX-B (4B1)	117	24 CLEARA- (5D1)
	14 E808-I (3C1)	53	118 +5V	25 GND 8 (5D1)
	15 E809-I (3B1)	54 CDCX-B (4A1)	119	26 PICK-A (5C1)
	16 E810-I (3B1)	55 GND	120	27 GND 8 (5C1)
	17 E811-I (3B1)	56 DCEX-B (4B4)	121 +5V	28 ITR- (5D4)
	18 E812-I (4B4)	57 GND	122 GND	29 GND 8 (5D4)
	19 E813-I (4C4)	58 TAKX-I (4B4)		30 IPF- (5D4)
B	20	59 GND	J2	31 GND 8 (5D4)
	60 DESX-B (4A4)		1 R0W09- (2D4)	32 GND 8 (5D4)
	61		2 GND 6 (2A4)	33 IHE- (5D4)
	62		3 R0W08- (2C4)	34 GND 8 (5C4)
	63		4 GND 6 (2A4)	35 READY- (5C4)
	64 E800+ (2D1)		5 R0W07 (2C4)	36 GND 8 (5C4)
	65 E800- (2D1)		6 GND 6 (2A4)	37 CI- (5C4)
	66 E801+ (4D4)		7 R0W06- (2B4)	38 GND 8 (5C4)
	67 E801+ (2C1)		8 GND 6 (2A4)	39 INDEX- (5B4)
	68 E801- (2C1)		9 R0W05- (2B4)	40 GND 8 (5B4)
A	69 E811+ (4D4)		10 GND 6 (2A4)	41
	70 E802+ (2C1)		11 R0W04- (2A4)	42
	71 E802- (2C1)		12 GND 6 (2A4)	43

CODE IDENT NO.	SIZE	DWG NO.	REV
21101	C	91C0455	C
SCALE		SHEET 6 OF 3	

COMPONENT MAP



-INDICATES NO VOLTAGE
OR GROUND ETCHED TYP

CODE	BRKT NO.	SIZE	DRAW NO.	
21101	C		91C0455	C
SCALE	SHEET 7 OF 2			

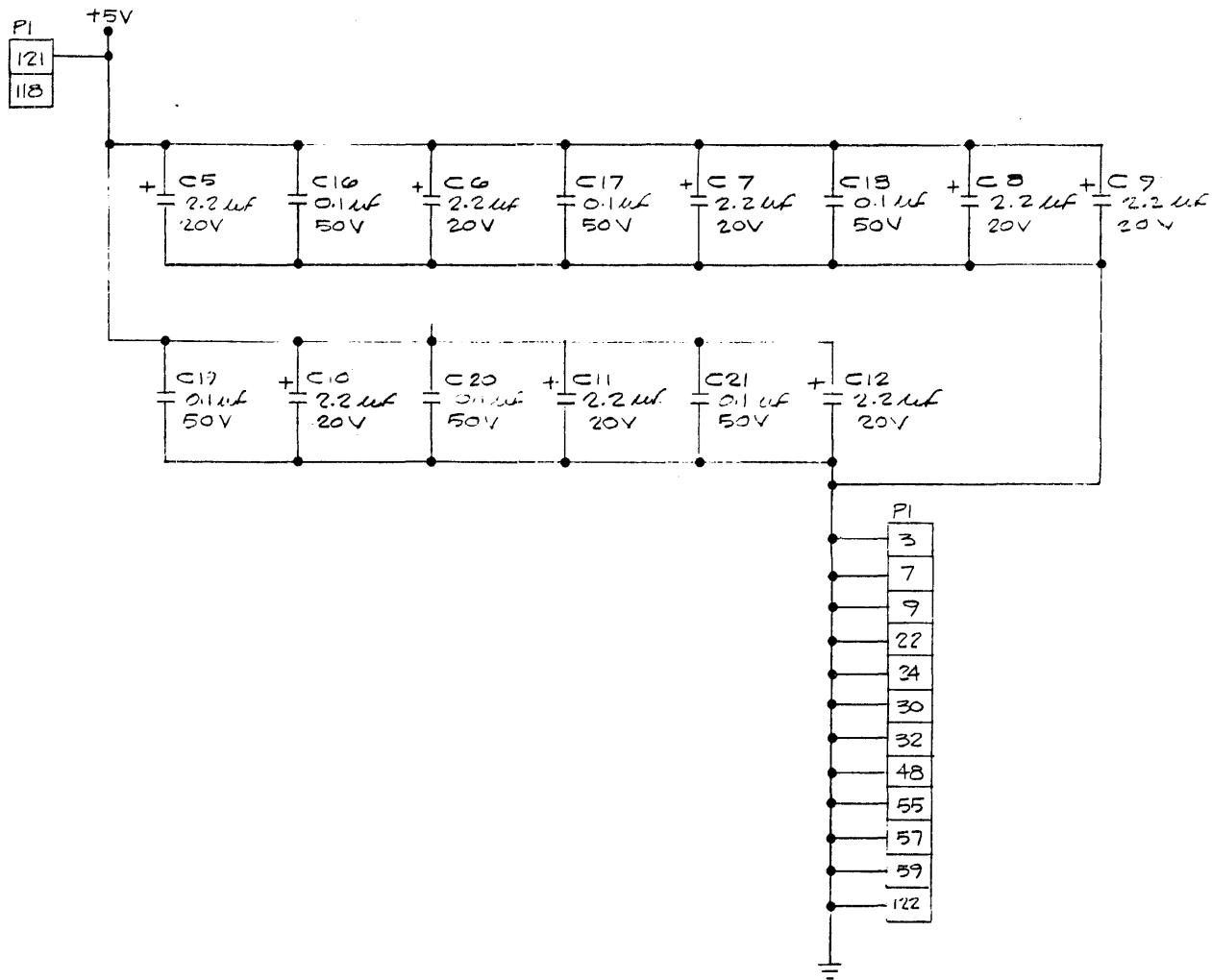
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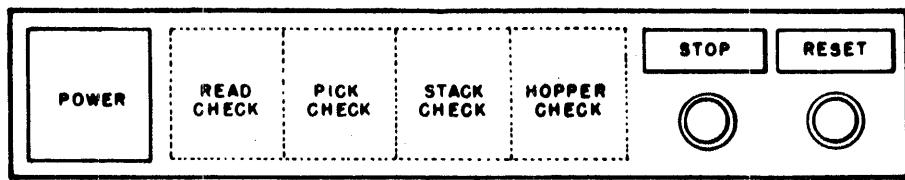
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D

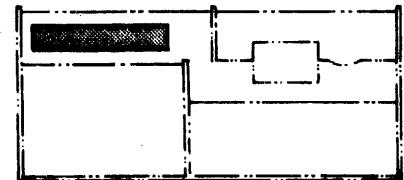


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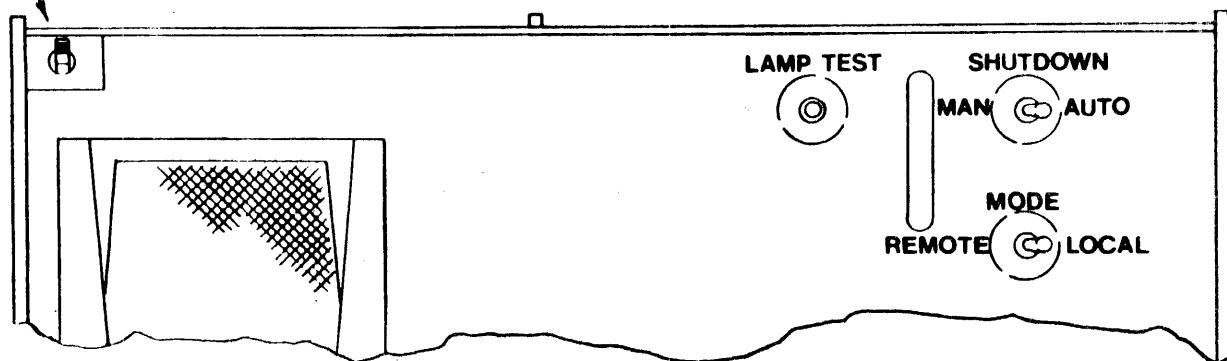
CODE IDENT NO.	SIZE	DWG NO	REV
21101	C	91CO455	C
SCALE	SHEET 1 OF 2		



FRONT CONTROL PANEL



AC POWER SWITCH



REAR PANEL

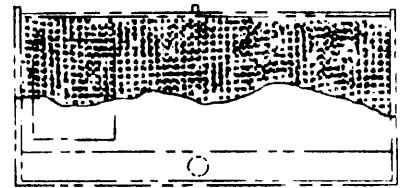


Figure 3. Switch Location

when the input hopper is empty. The motors will automatically restart when cards are placed in the hopper and the RESET switch is depressed. Expect a delay of approximately 3 seconds for the motors to run up.

OPERATIONAL FLOW CHART

Figure 4 shows a flow chart of the sequence of events which may be encountered in operating the reader. If trouble is experienced, refer to this check list before calling for maintenance.

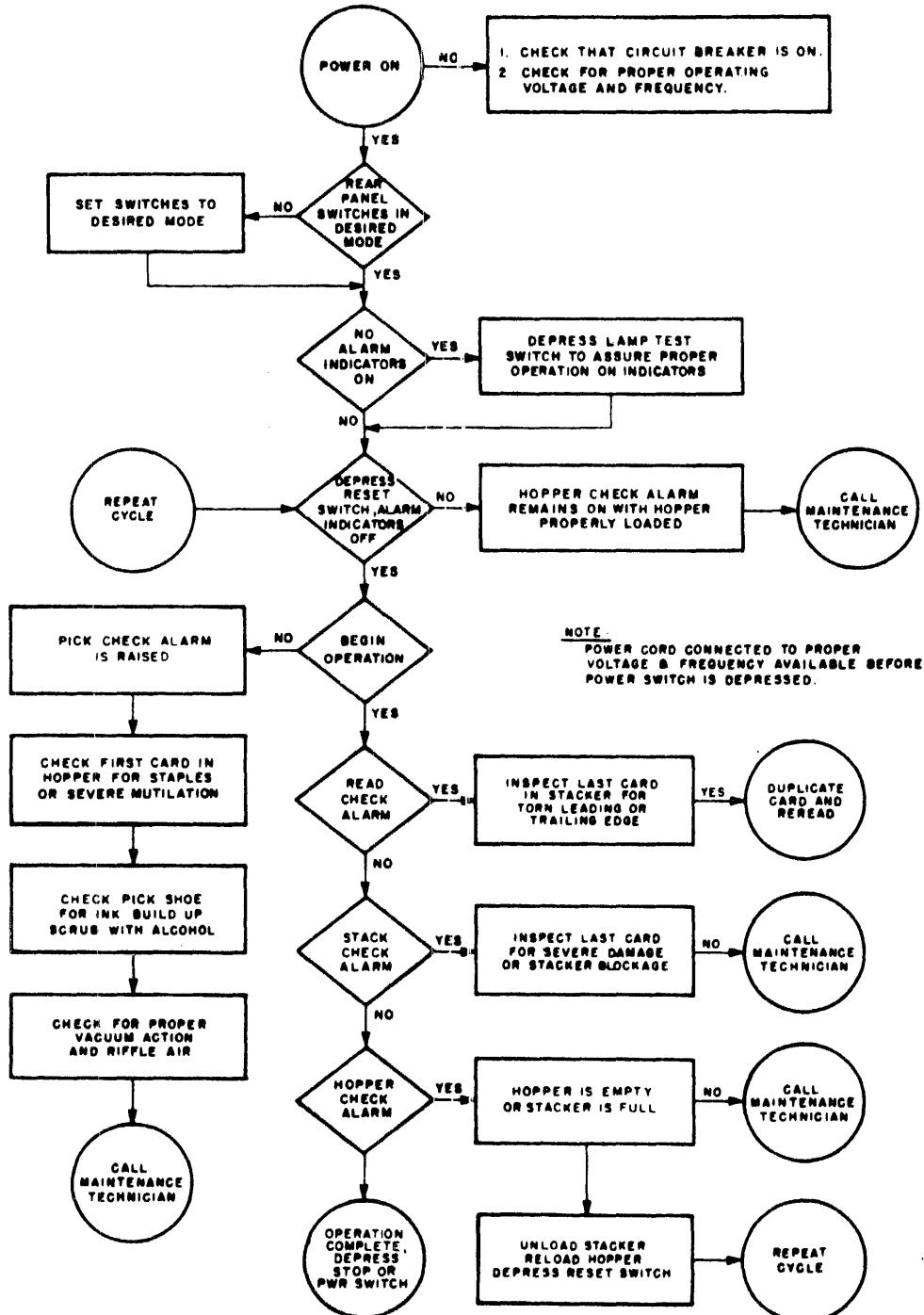


Figure 4. Operational Flow Chart

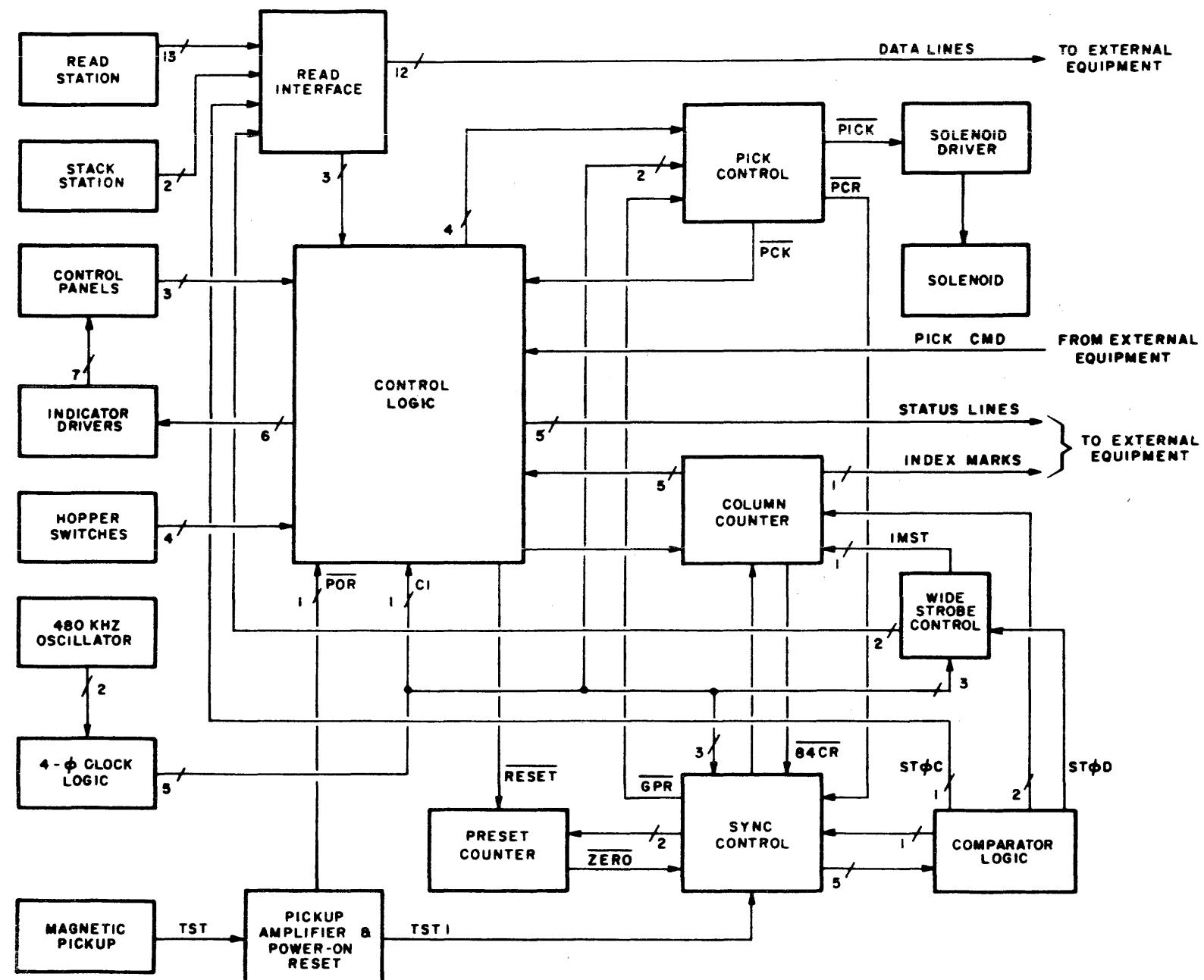


Figure 5. M Series Card Reader Logic Block Diagram

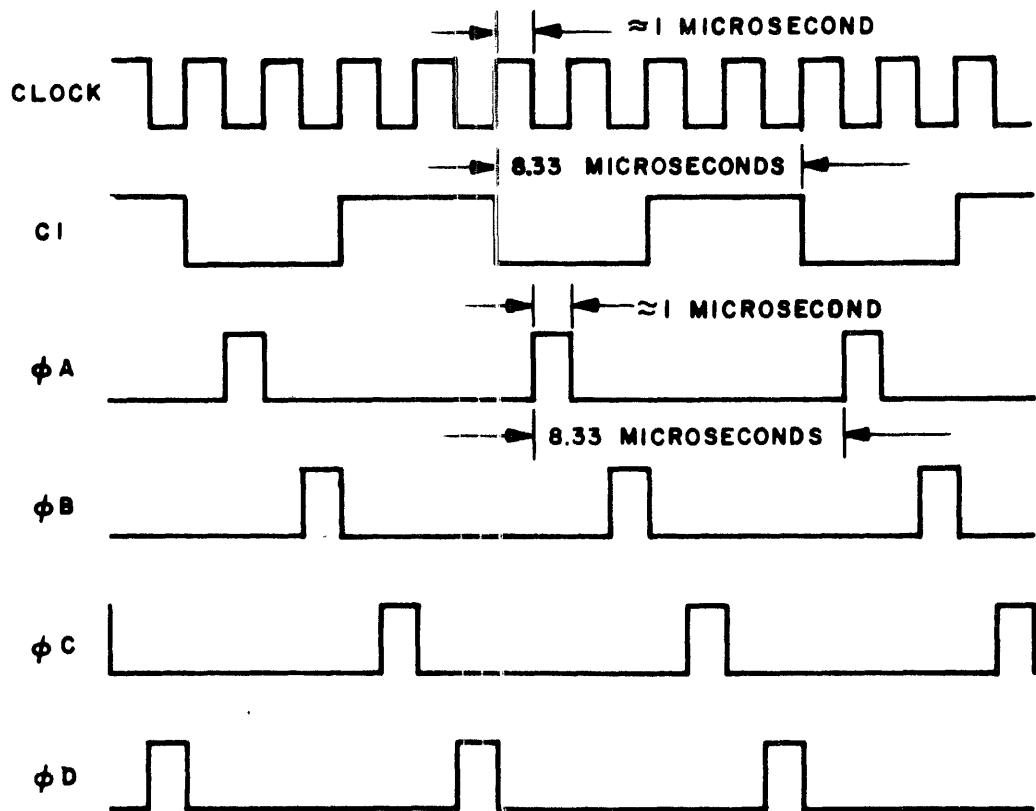
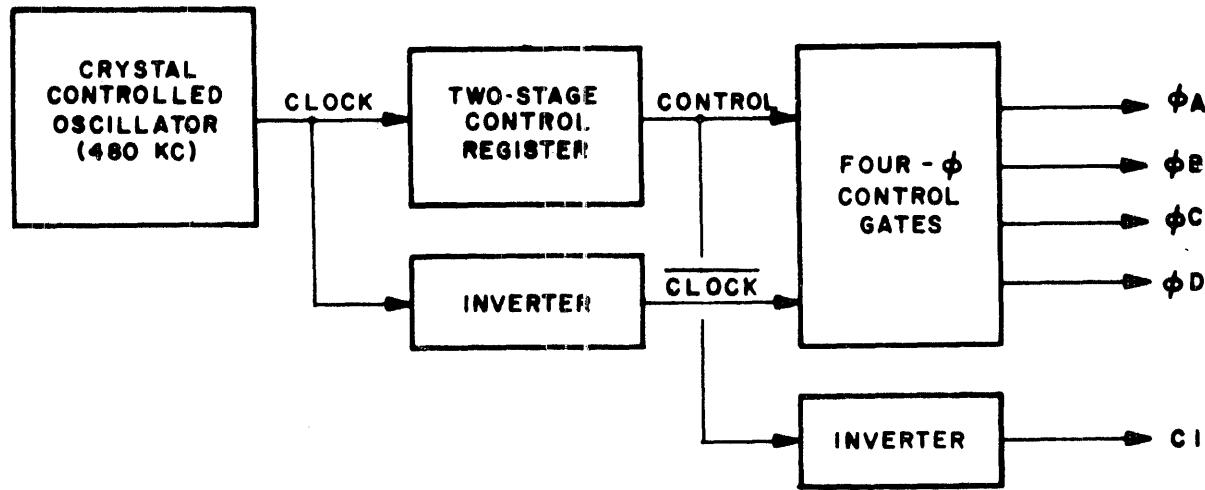
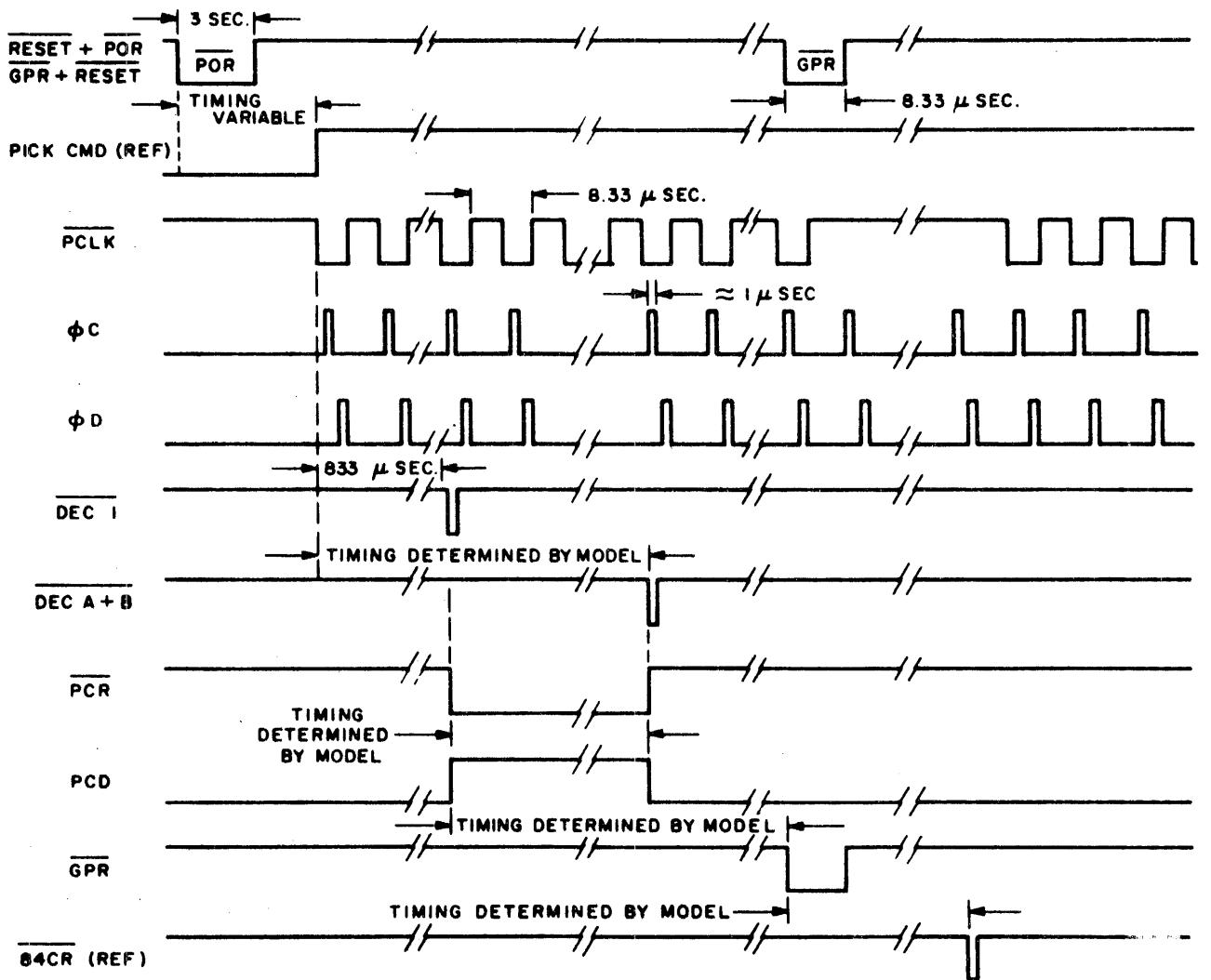
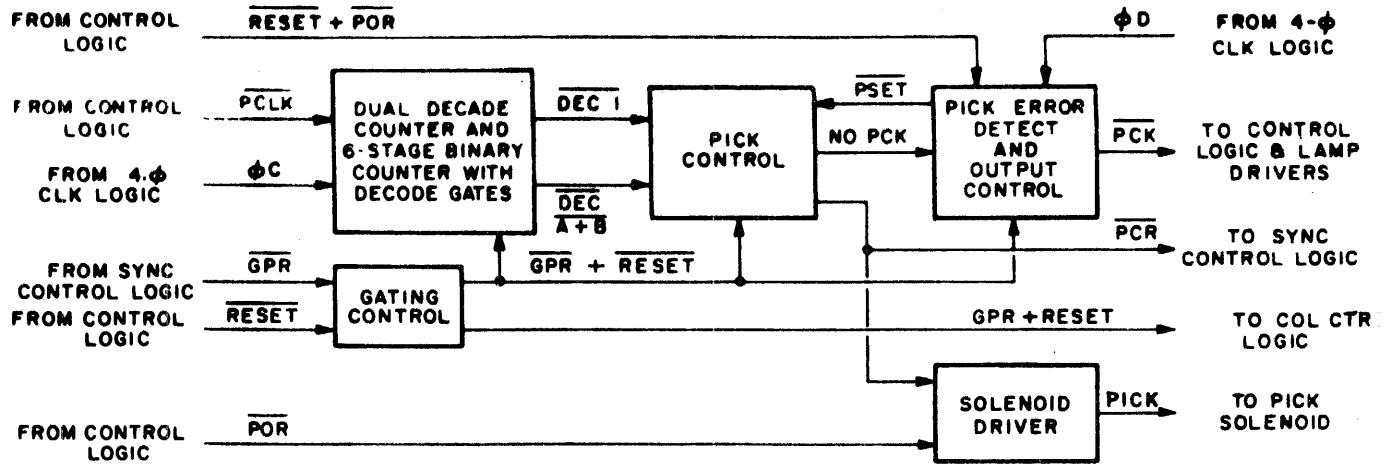
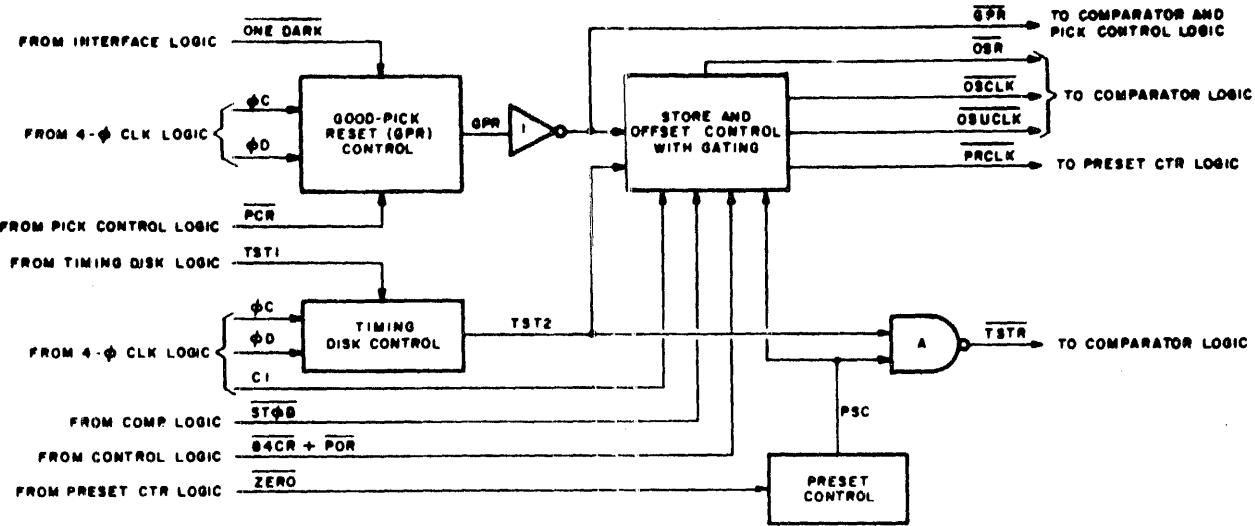


Figure 7. Oscillator/Four-Phase Clock Logic Block Diagram



NOTE: TIMING NOT SHOWN TO SCALE.

Figure 8. Pick Control Logic Block Diagram



NOTES.

- (1) FOLLOWING TIMING NOT SHOWN TO SCALE.
- (2) TIME SCALE OF SECOND GROUP NOT SAME AS FIRST GROUP

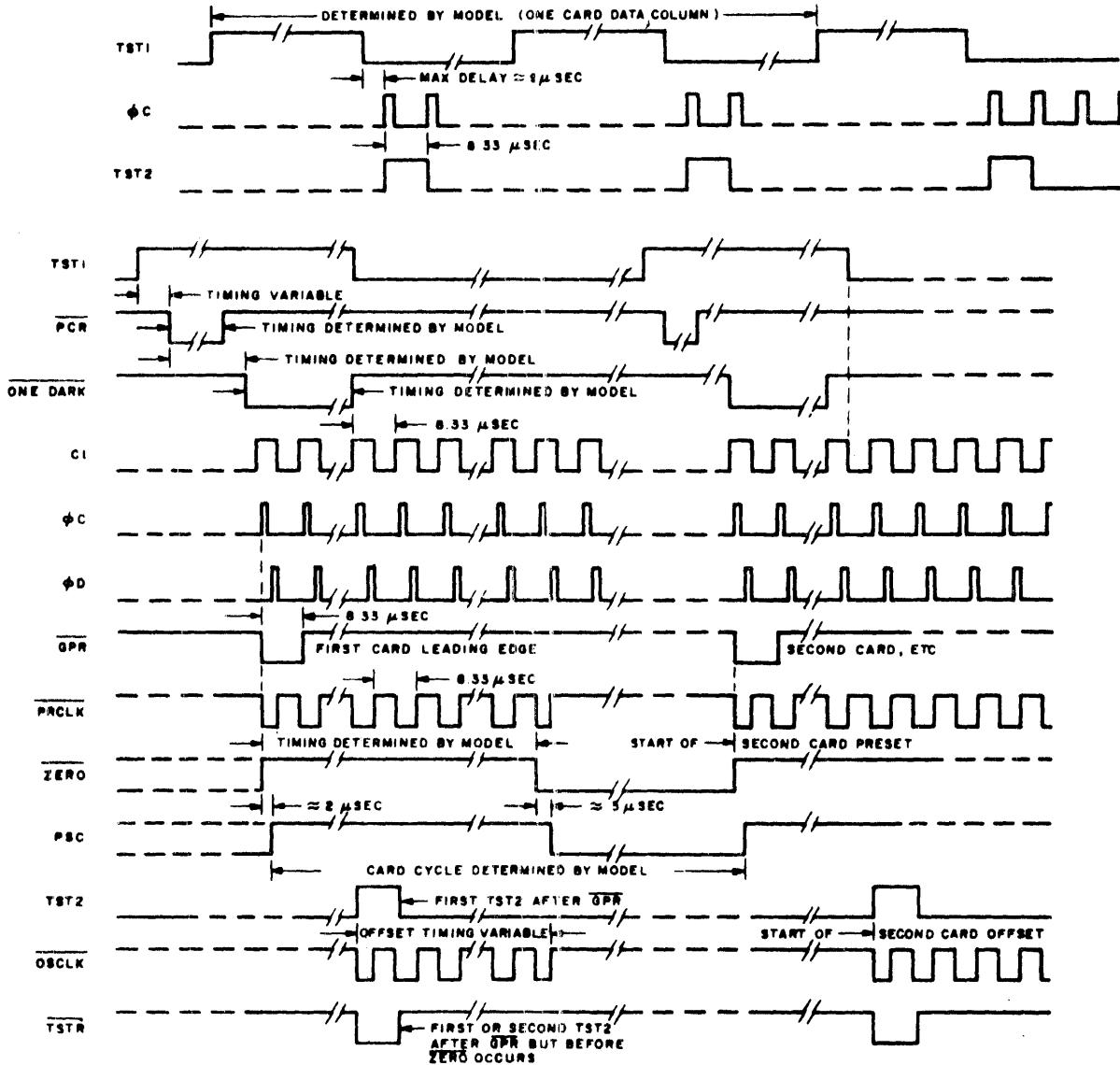


Figure 9. Sync Control Logic Block and Timing Diagram
(Sheet 1 of 2).

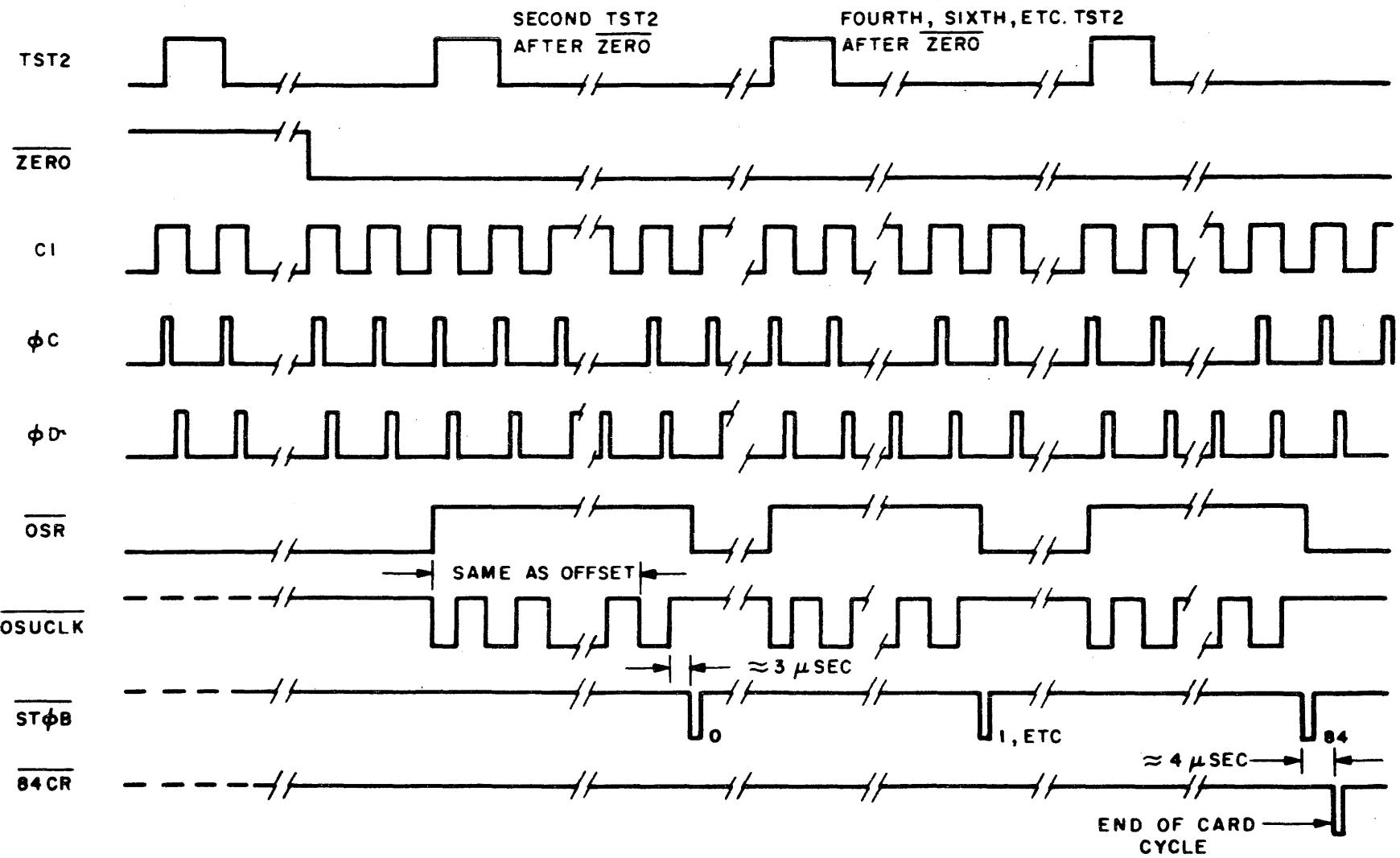
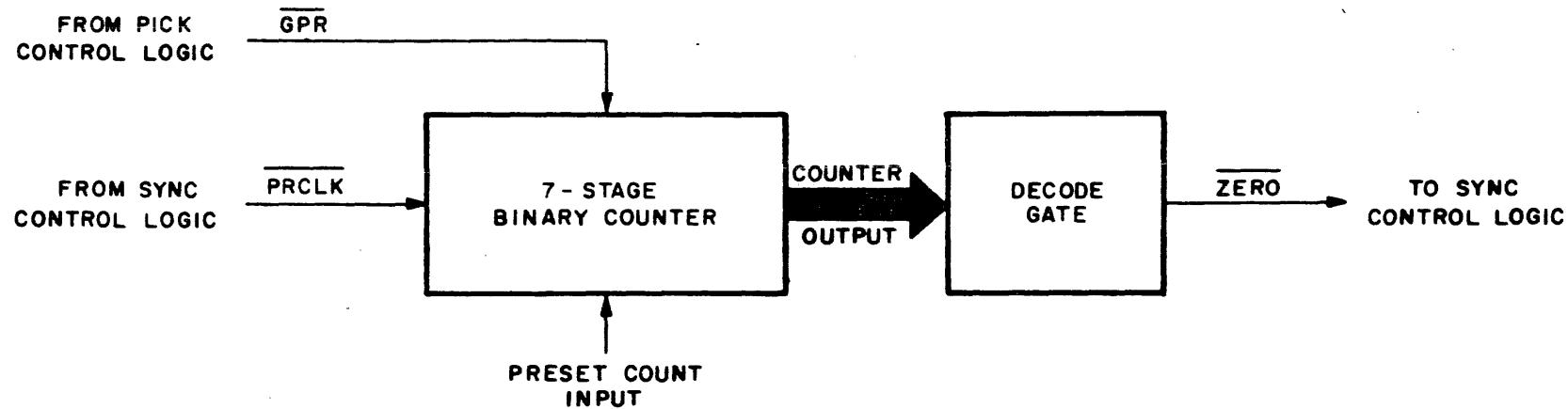


Figure 9. Sync Control Logic Block and Timing Diagram
(Sheet 2 of 2)



- 20 -

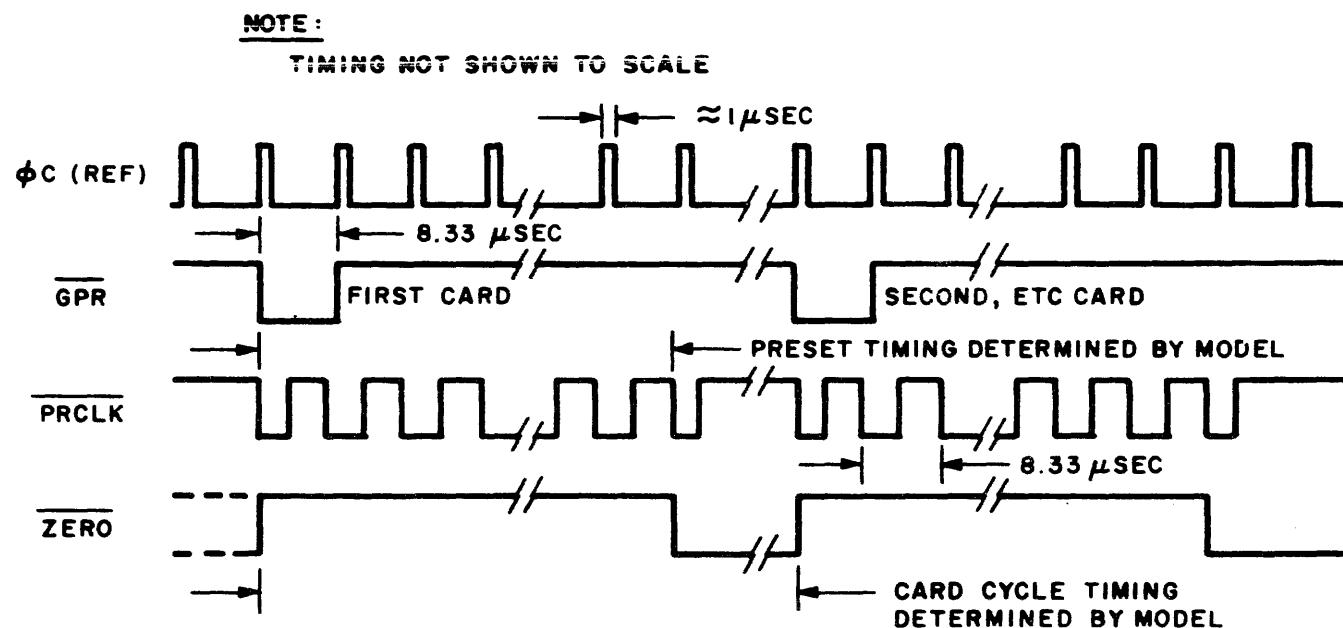


Figure 10. Preset Counter Logic Block Diagram

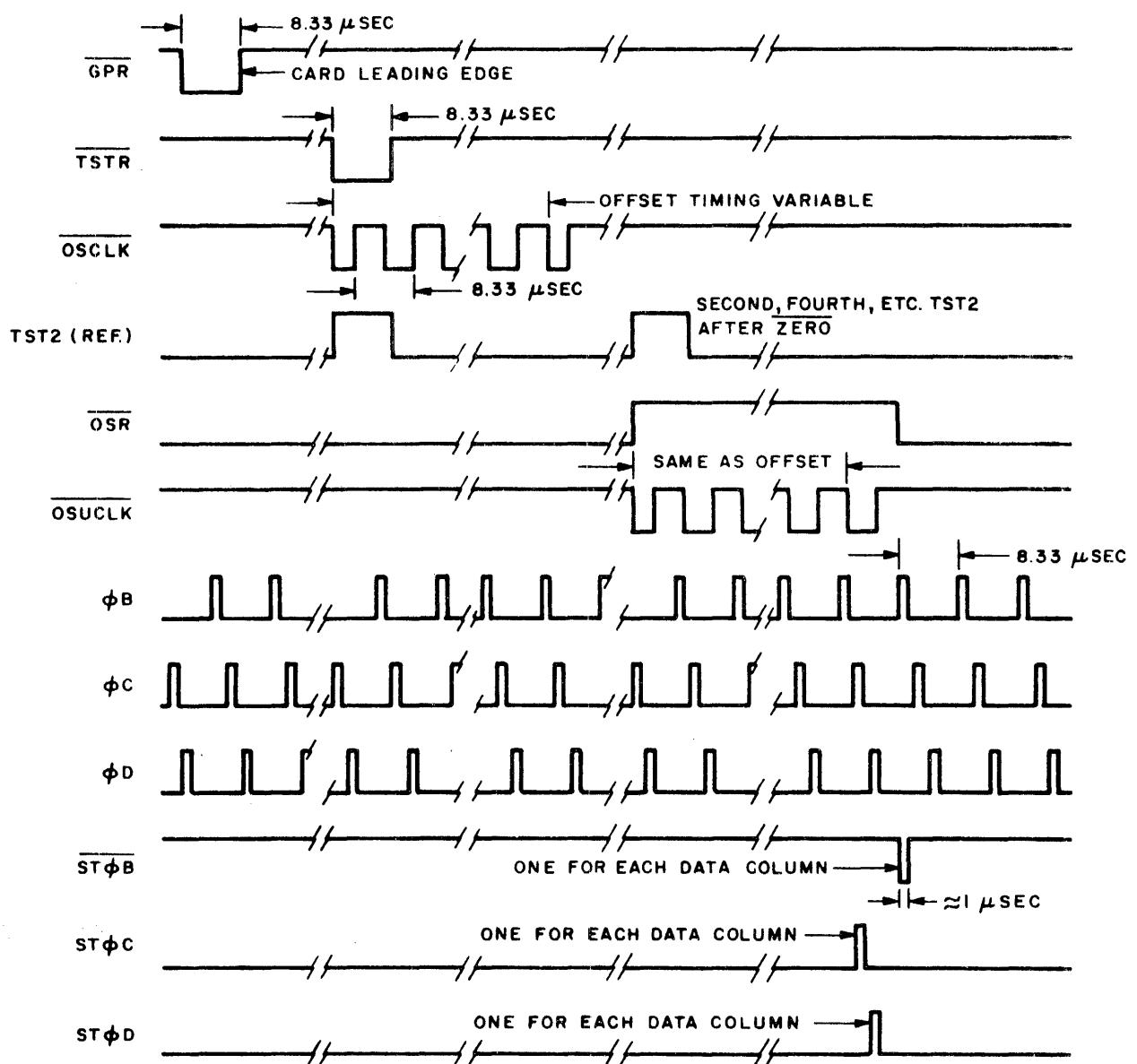
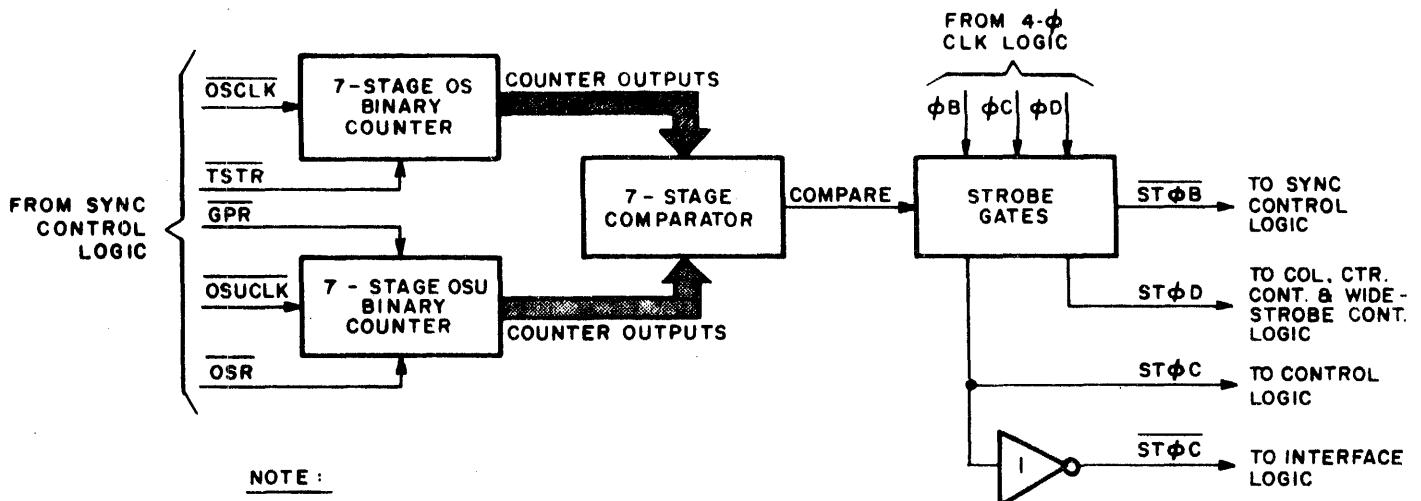
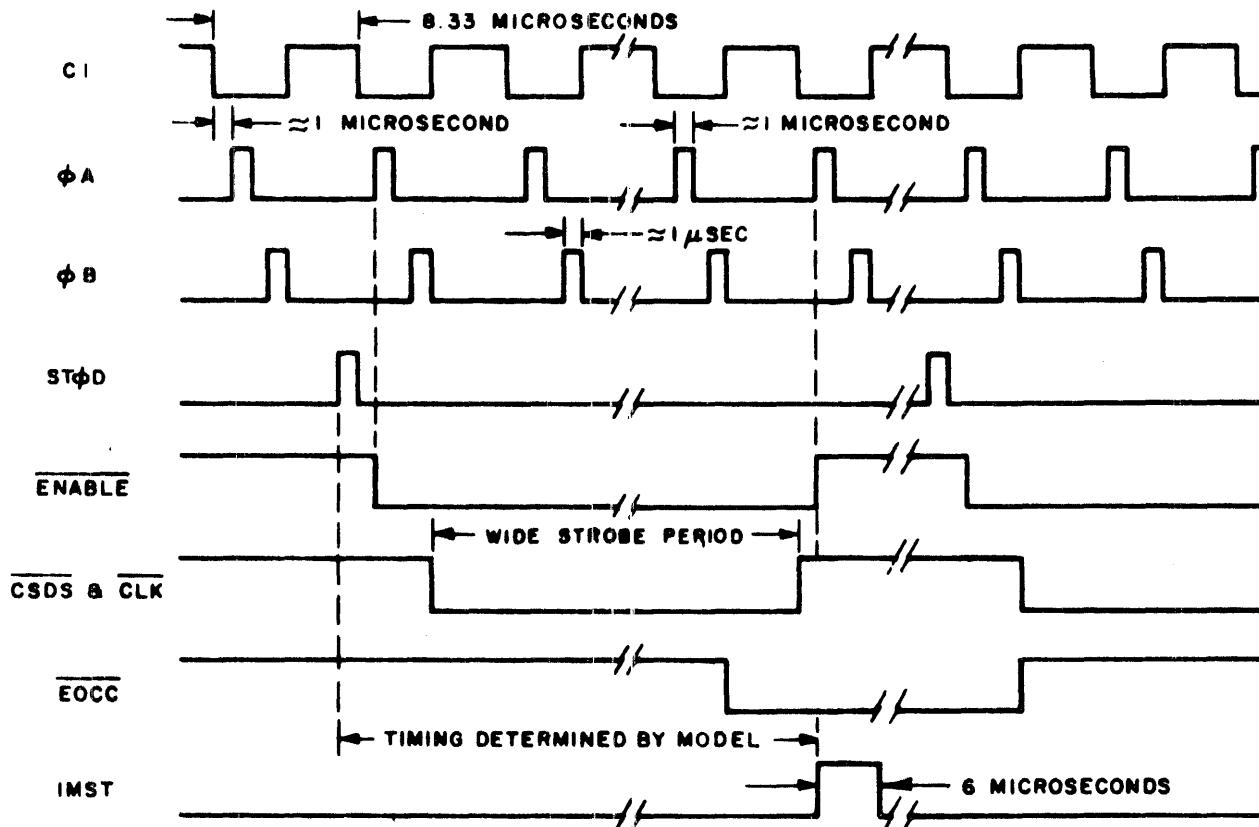
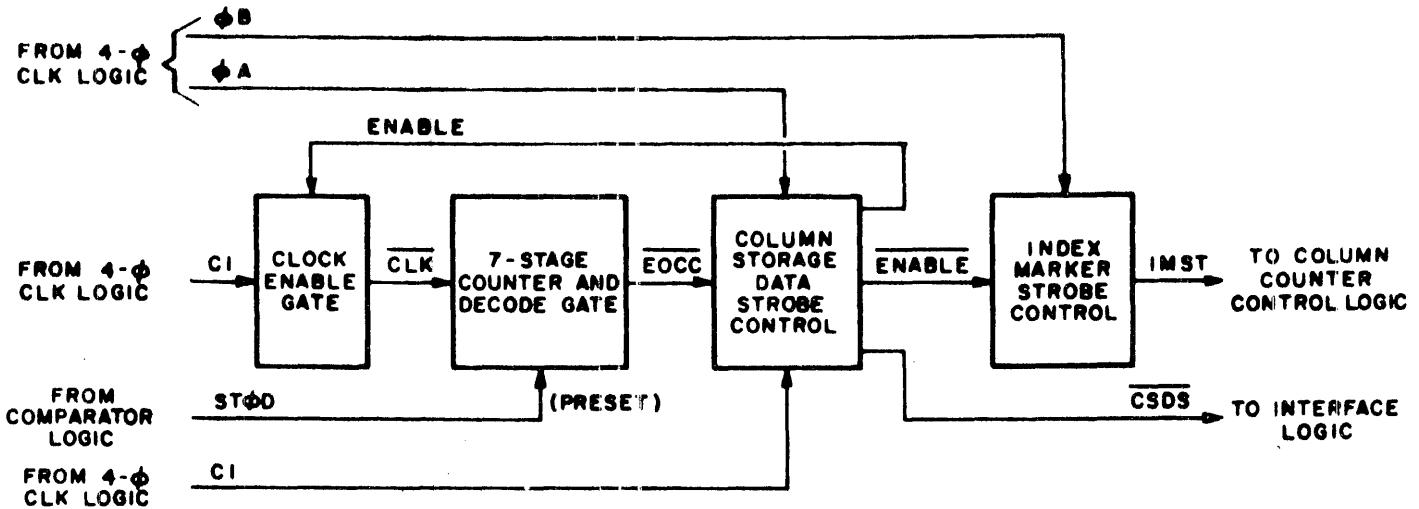


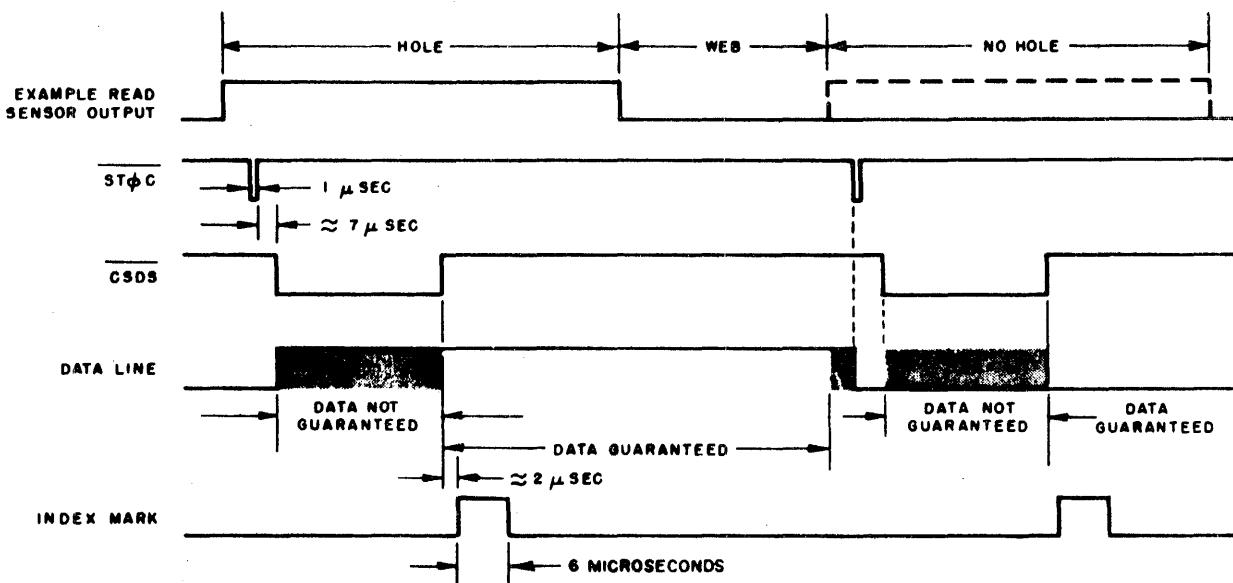
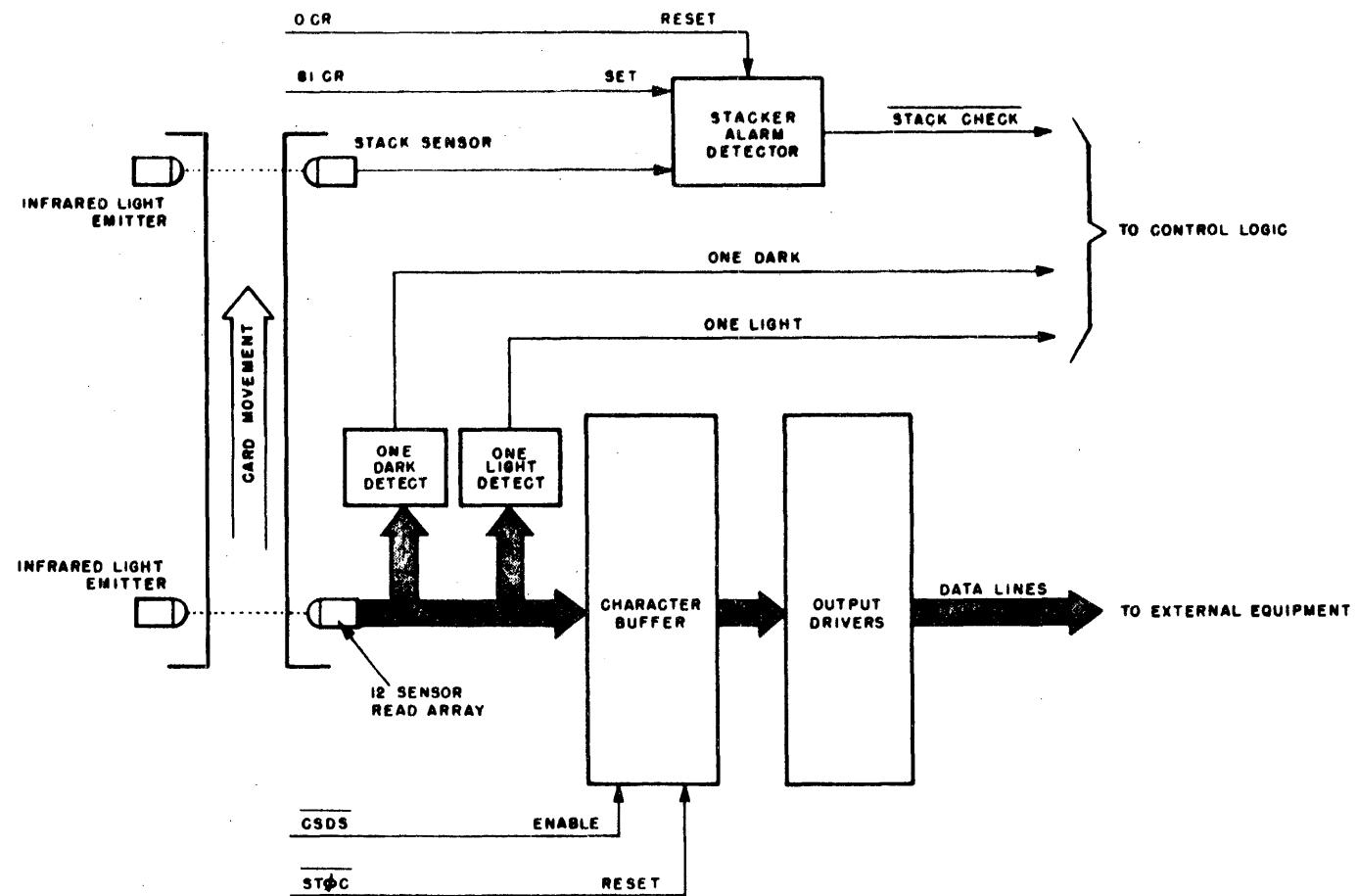
Figure 11. Comparator Logic Block Diagram



NOTES:

- (1) STΦD SYNCHRONIZED TO CARD DATA COLUMNS.
- (2) TIMING NOT SHOWN TO SCALE.

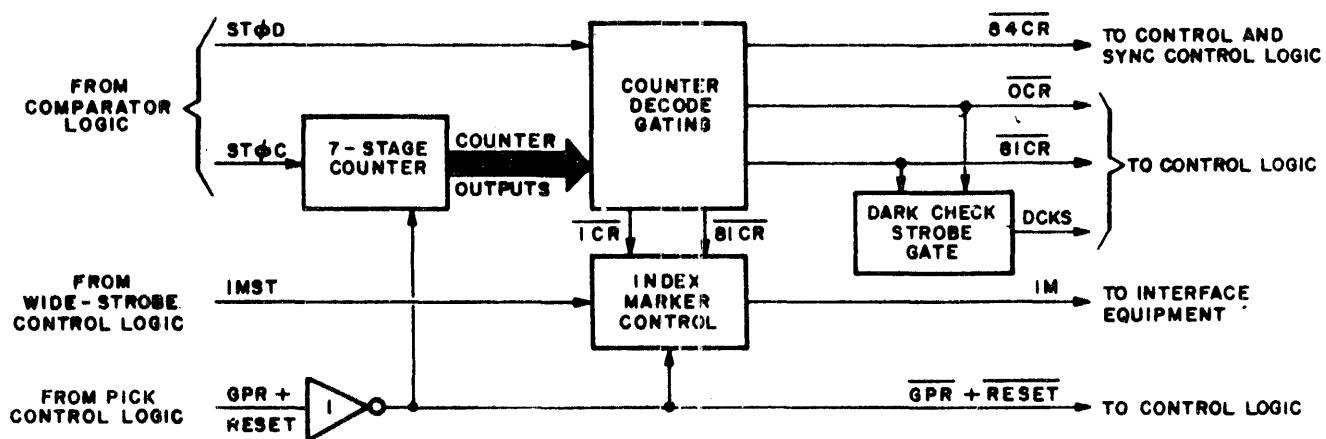
Figure 12. Wide-Strobe Control Logic Block Diagram



NOTES:

- (1) TIMING NOT SHOWN TO SCALE.
- (2) THE SPACING BETWEEN ST_φC, THE DURATION OF CSDS, AND THE GUARANTEE PERIOD OF THE DATA DIFFERS DEPENDING ON READER MODEL. REFER TO INTERFACE SECTION FOR SPECIFIC TIMING.

Figure 13. Character Buffer Storage Logic Block Diagram



NOTE :

- (1) TIMING NOT SHOWN TO SCALE.
- (2) GPR OCCURS AT LEADING EDGE OF CARD.

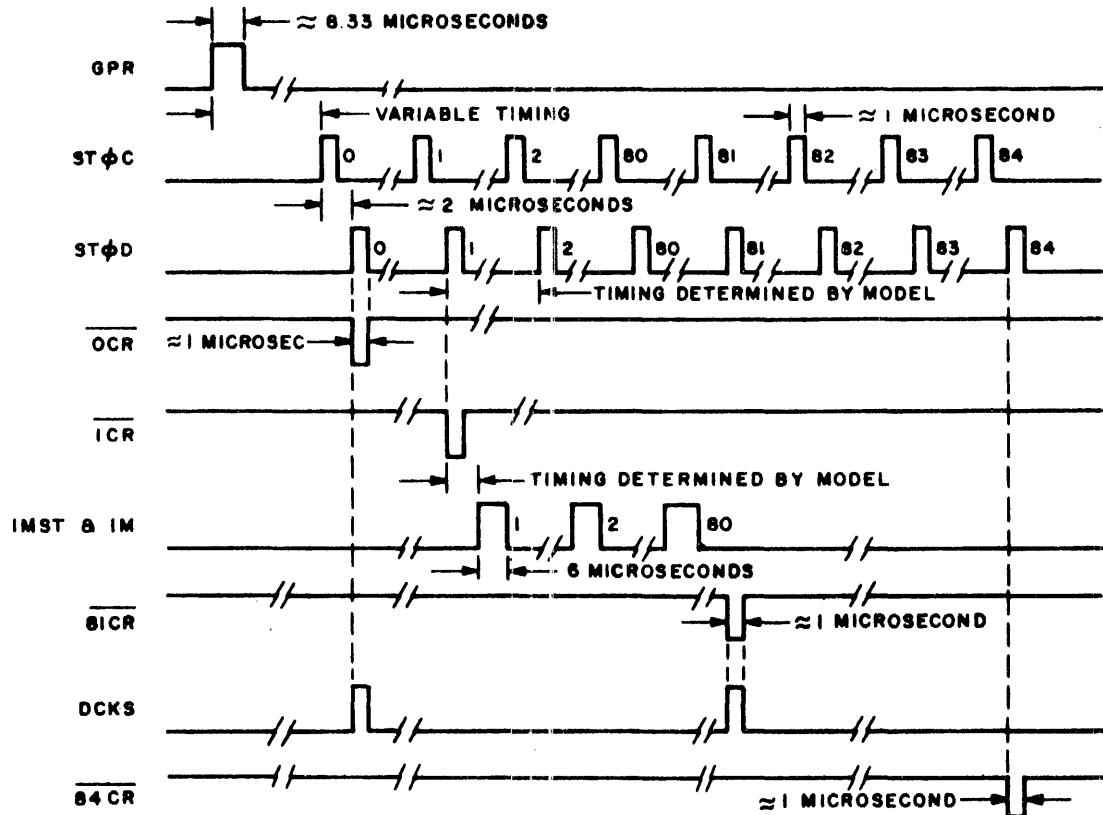
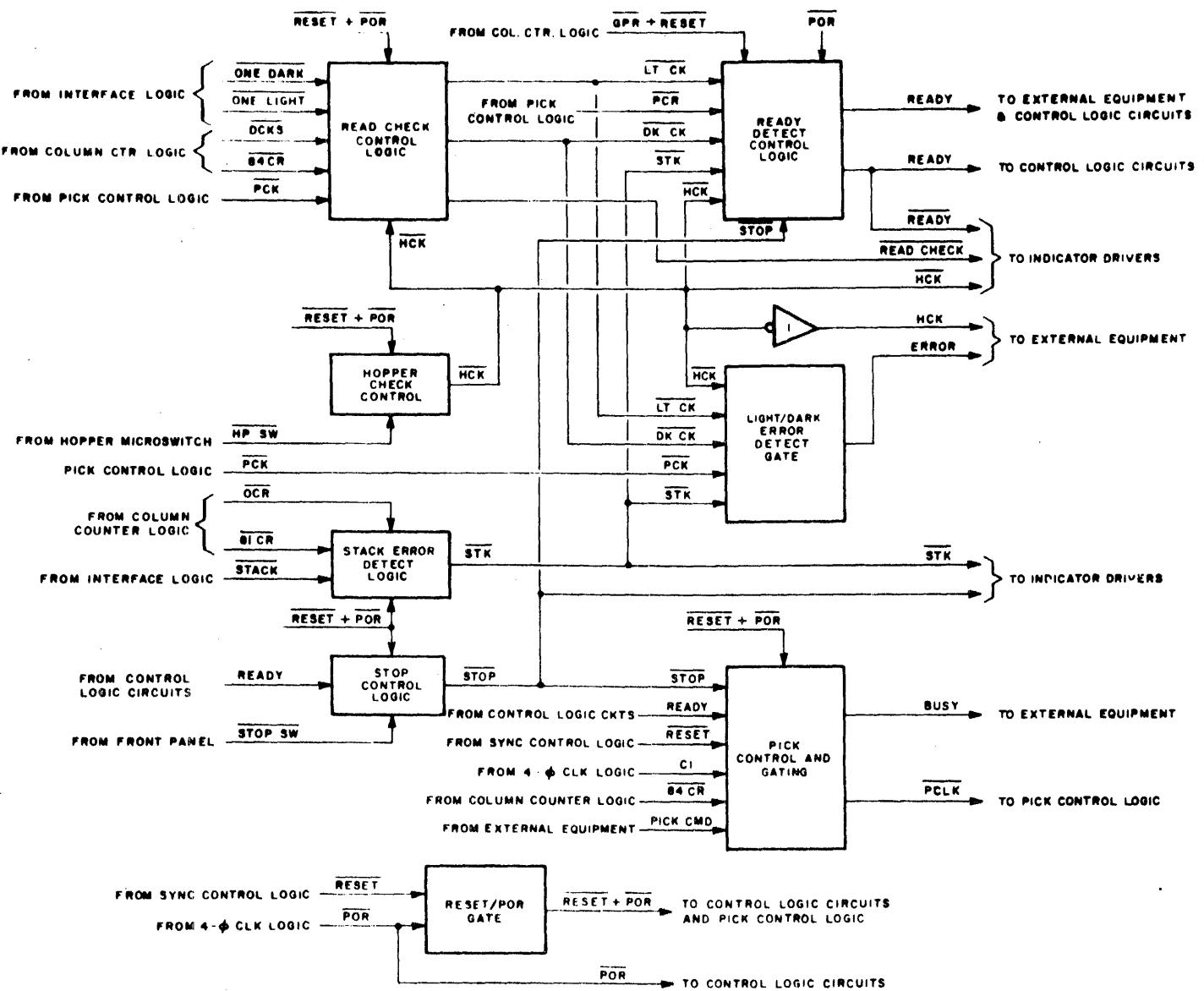


Figure 14. Column Counter Control Logic Block Diagram



NOTE:
TIMING NOT SHOWN TO SCALE

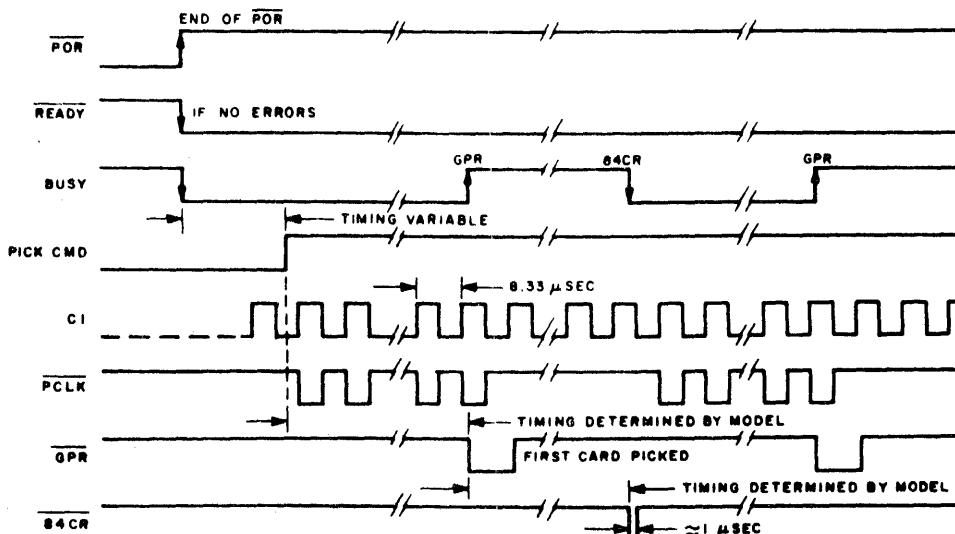
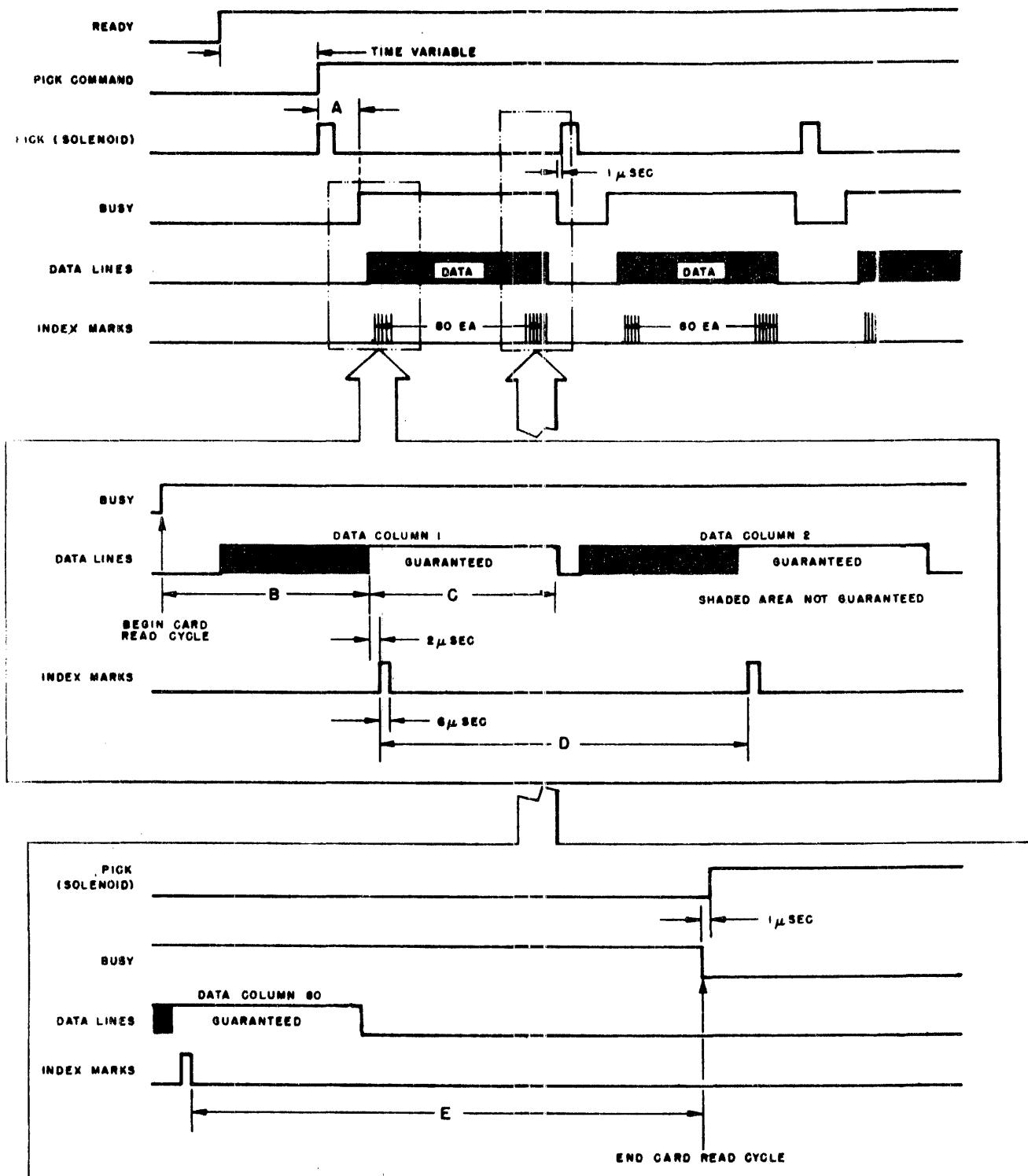


Figure 15. Control Logic Block and Timing Diagram



NOTE:
WAVEFORMS NOT
SHOWN TO SCALE.

MODEL	A (MIN)	B	C	D	E	CARD PICK CYCLE
M200	24	6250	1314	2014	8050	200
M300	24	2600	435	870	102,660	200
M600	24	2600	435	870	3480	100
M1000	16	1860	240	478	1910	60
M1600	14	1120	240	408	1520	50
	M SEC	μ SEC	μ SEC	μ SEC	μ SEC	M SEC

Figure 16. Standard Interface Timing for M Series Readers

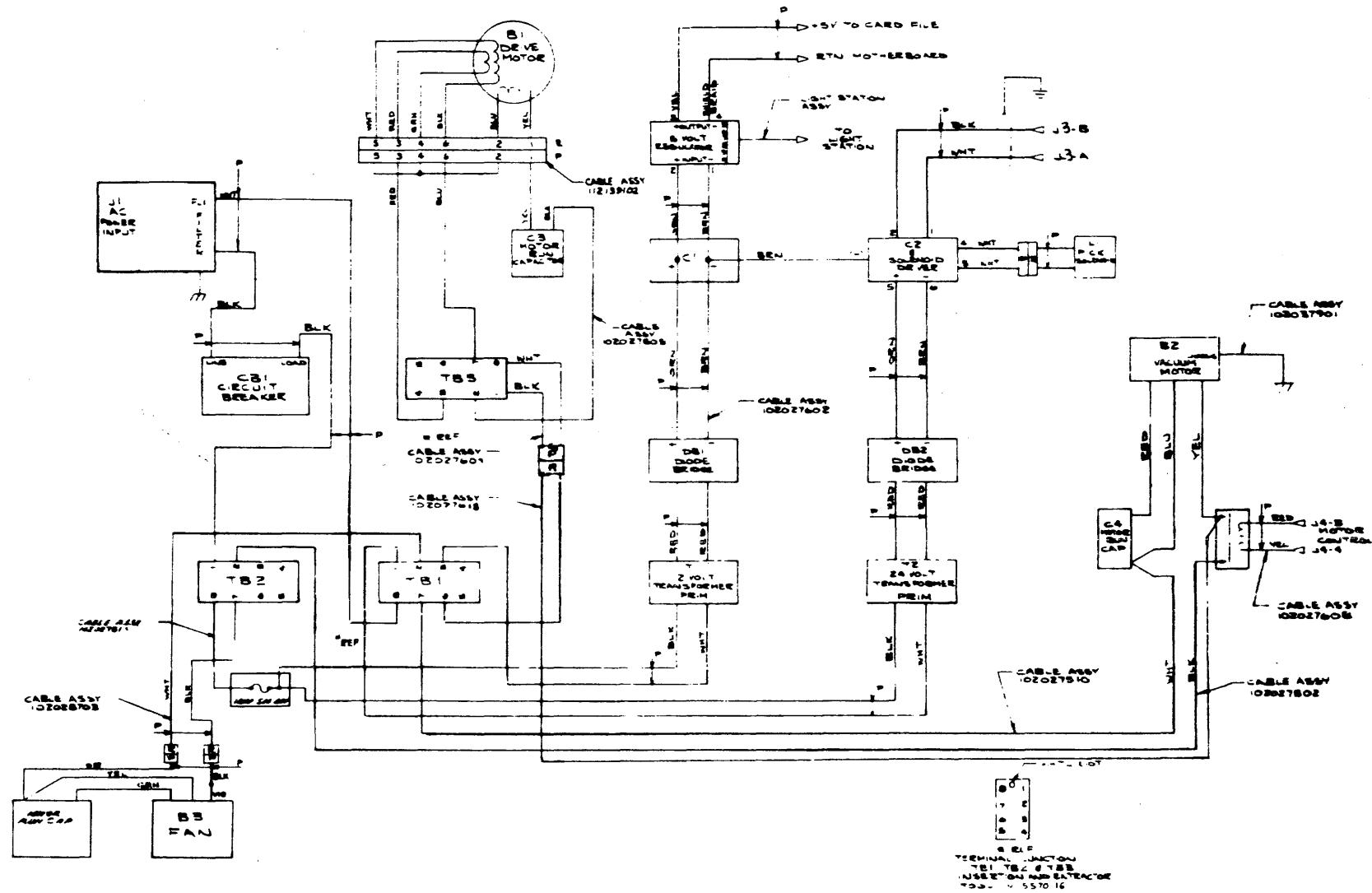


Figure A1A. Wiring Diagram, AC Power Distribution, 230 VAC, 50 Hz
Dwg. No. 1040819

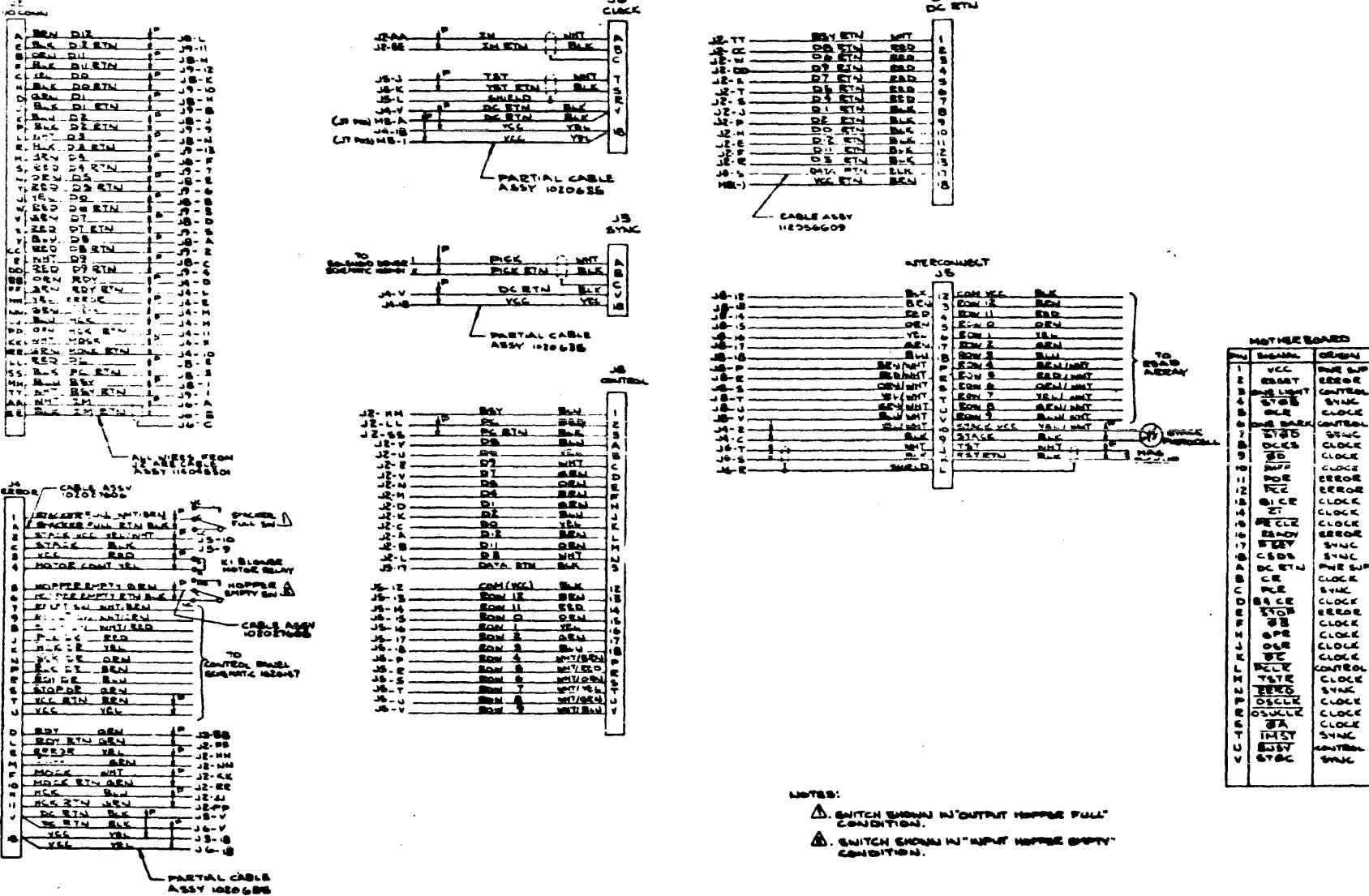


Figure A1. Wiring Diagram, Card Cage
(Dwg. No. 1141934) CS 139A

A3

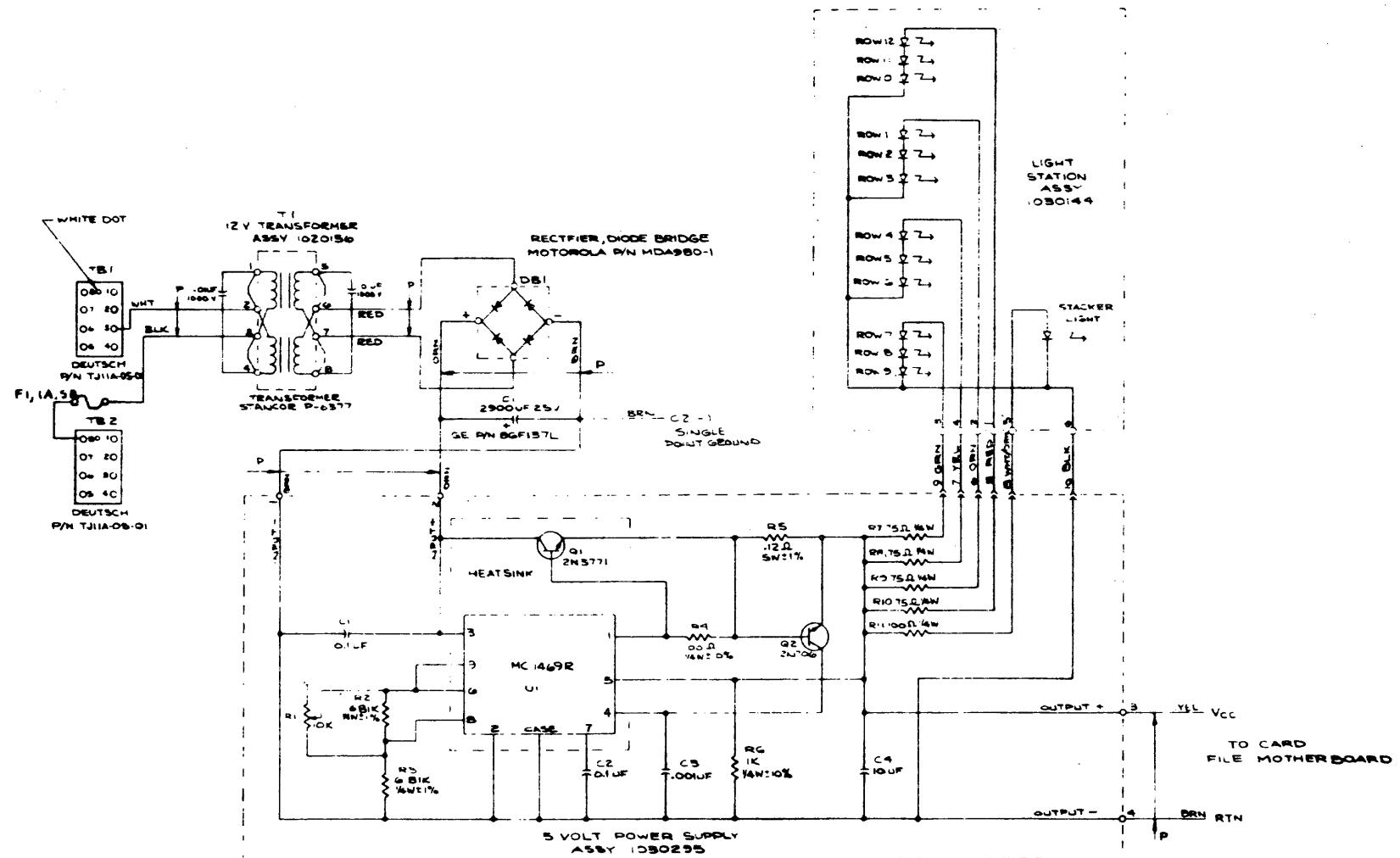


Figure A2. 5 Volt Power Supply
Dwg. No. 1140637

A2A

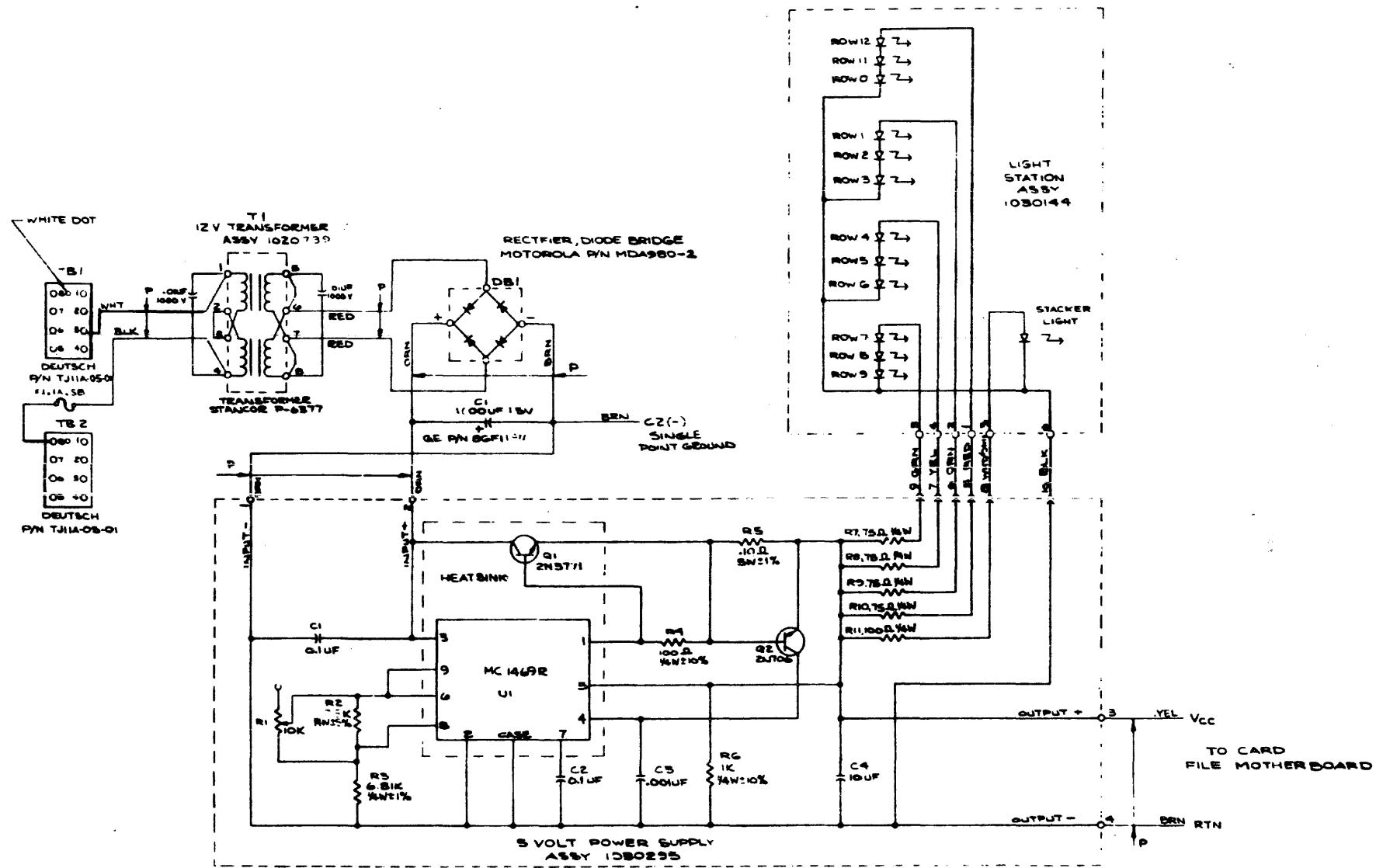


Figure A2A. 5 Volt Power Supply

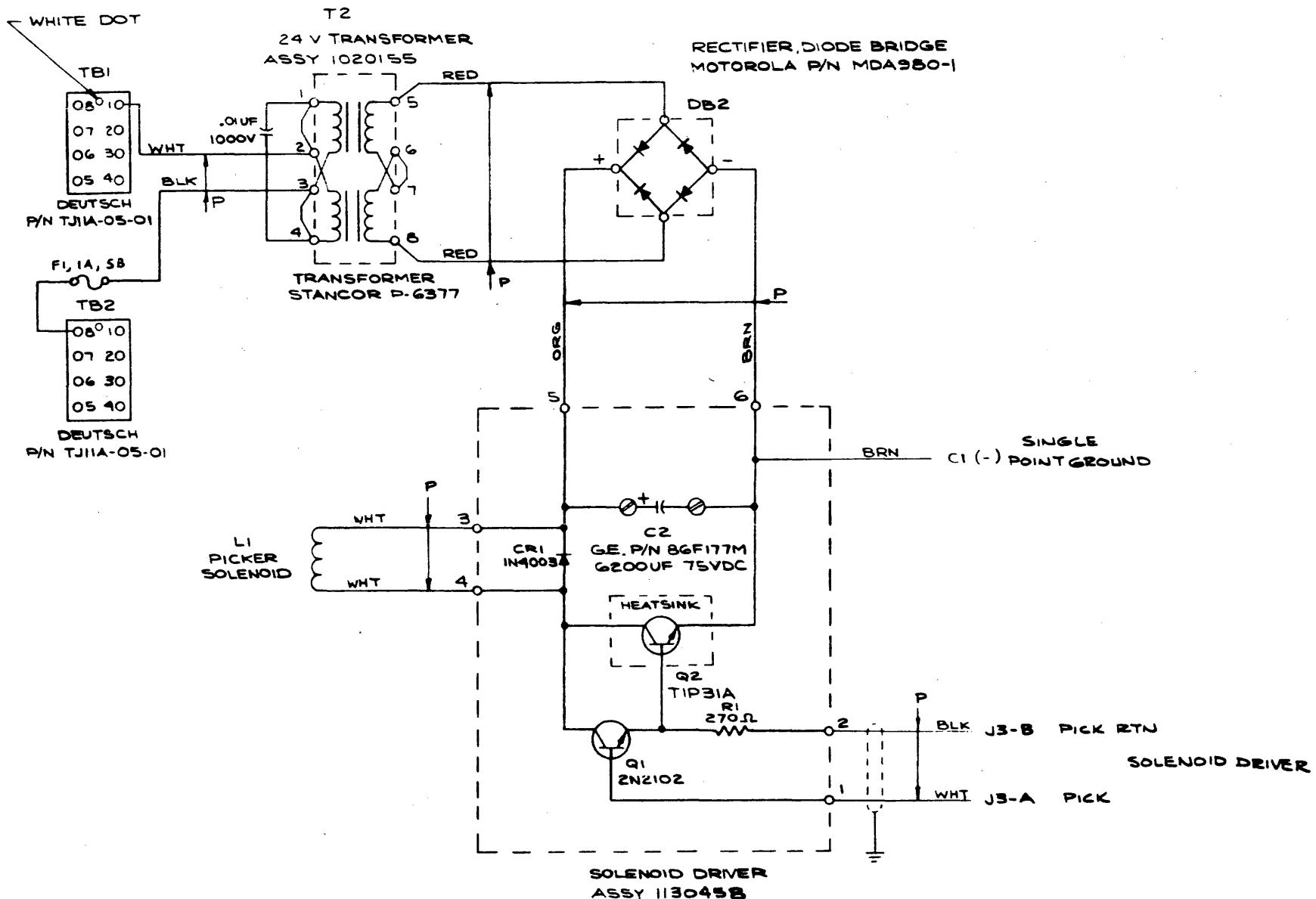


Figure A3. Solenoid Driver
Dwg. No. 1140623

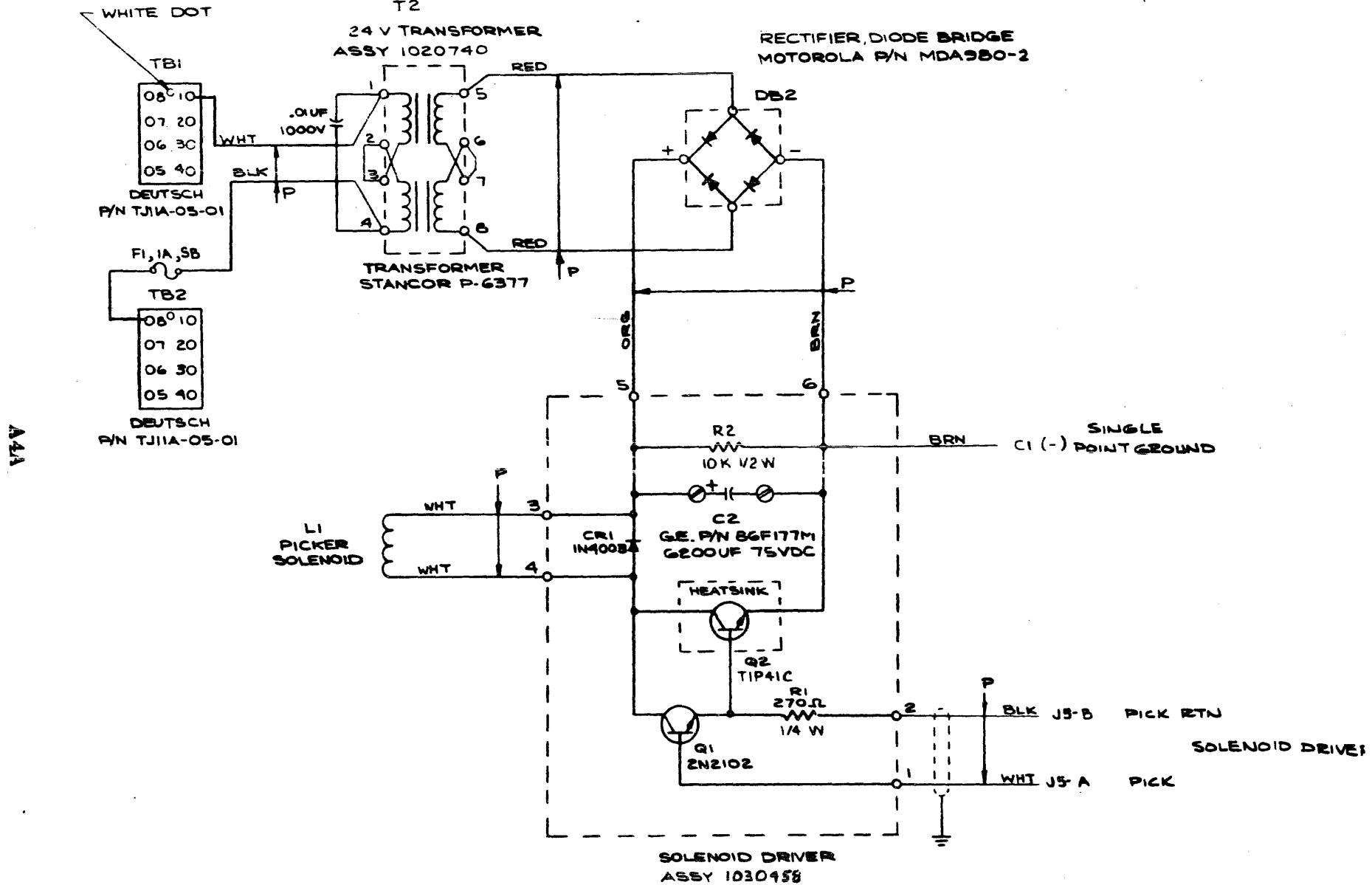
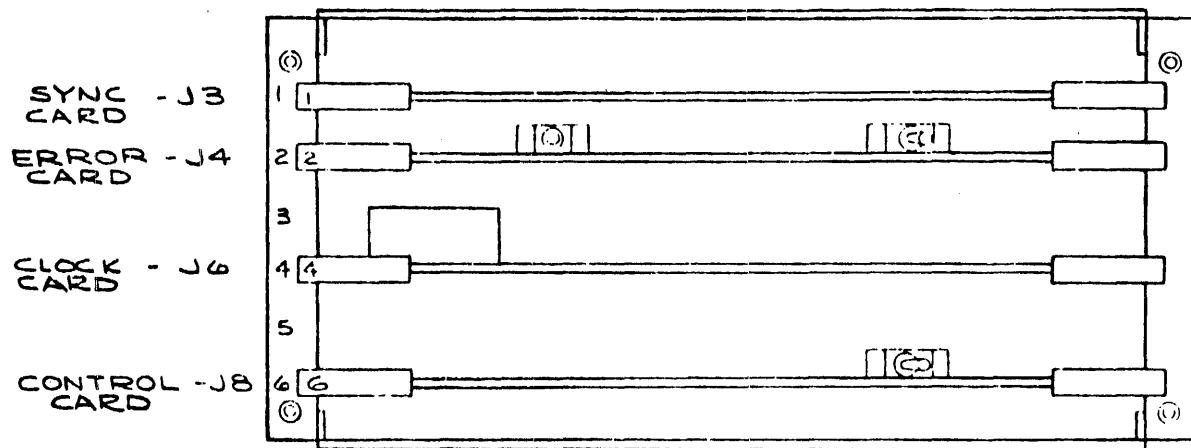
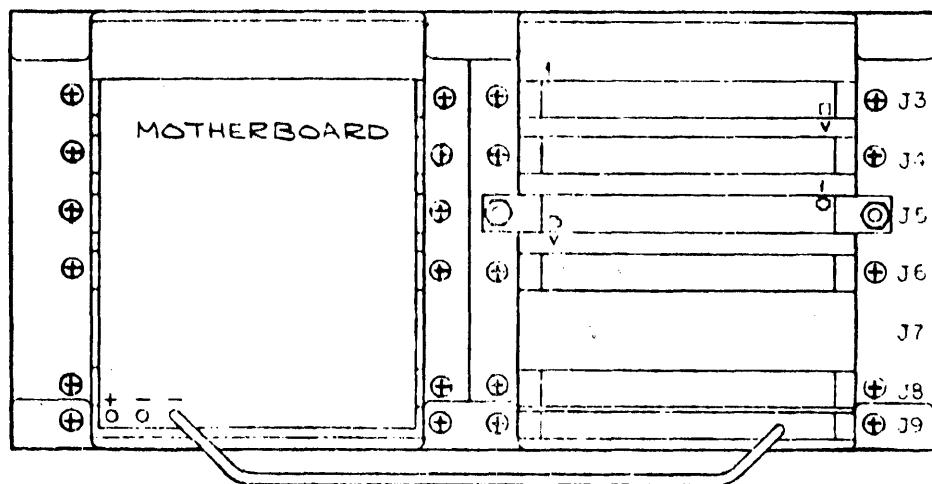


Figure A3A. Solenoid Driver



CARD FILE, REAR VIEW
COVER REMOVED



CONNECTOR VIEW

Figure A4. Card File

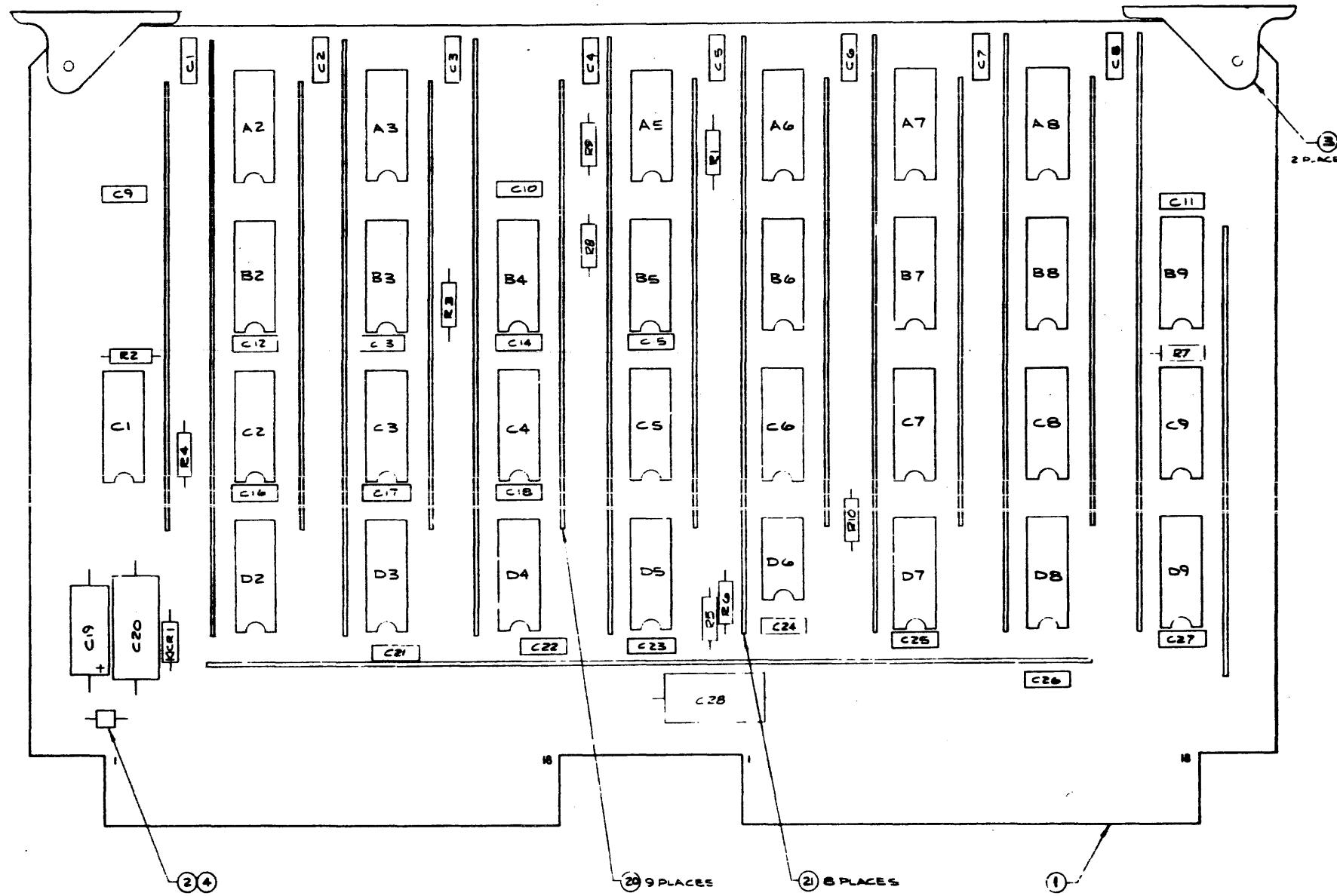


Figure A5. Sync Card Assembly
Dwg. No. 1040353

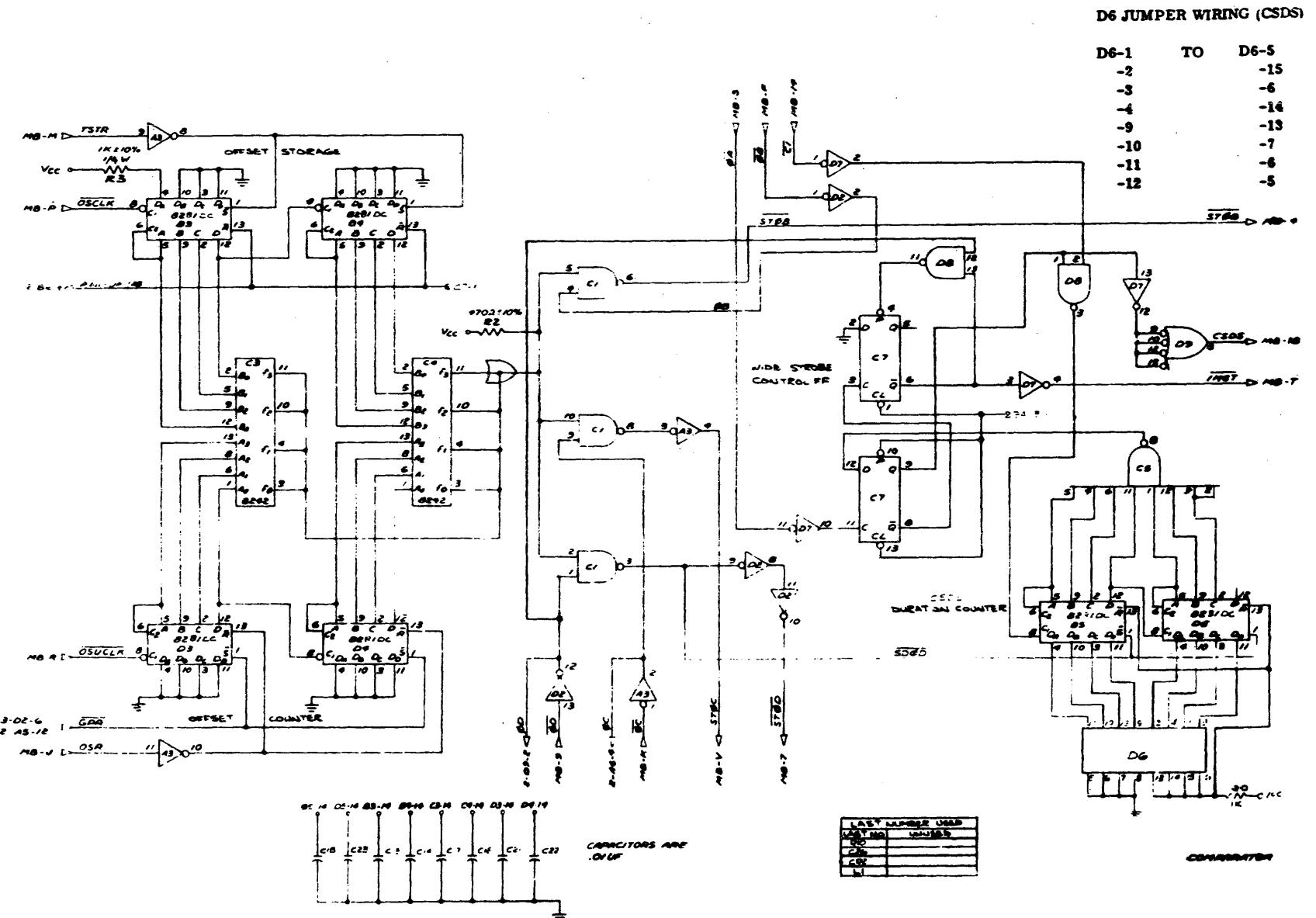


Figure A6. Sync Card Schematic Dwg. No. 1640943 (Sheet 1 of 3) (M-200)

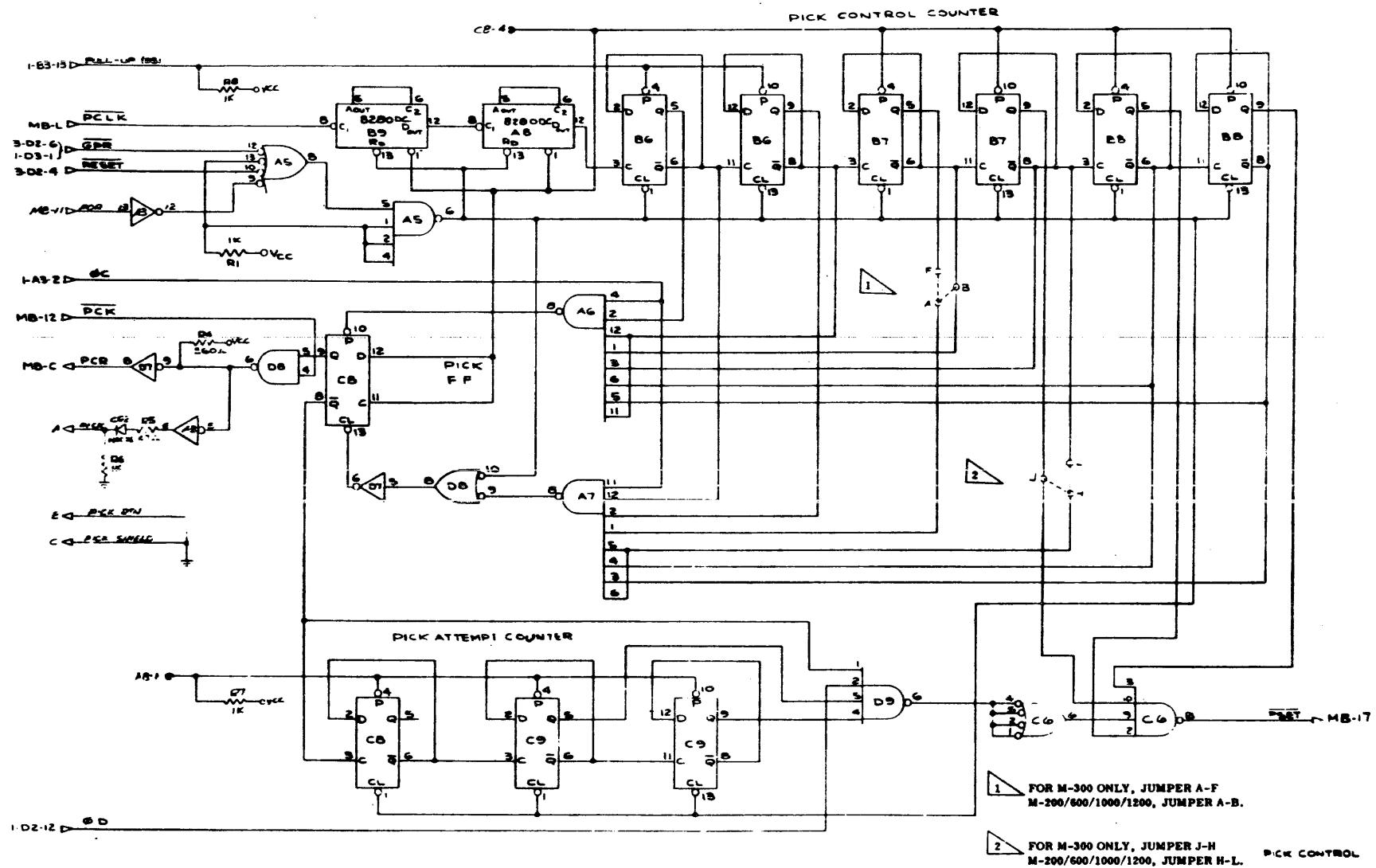
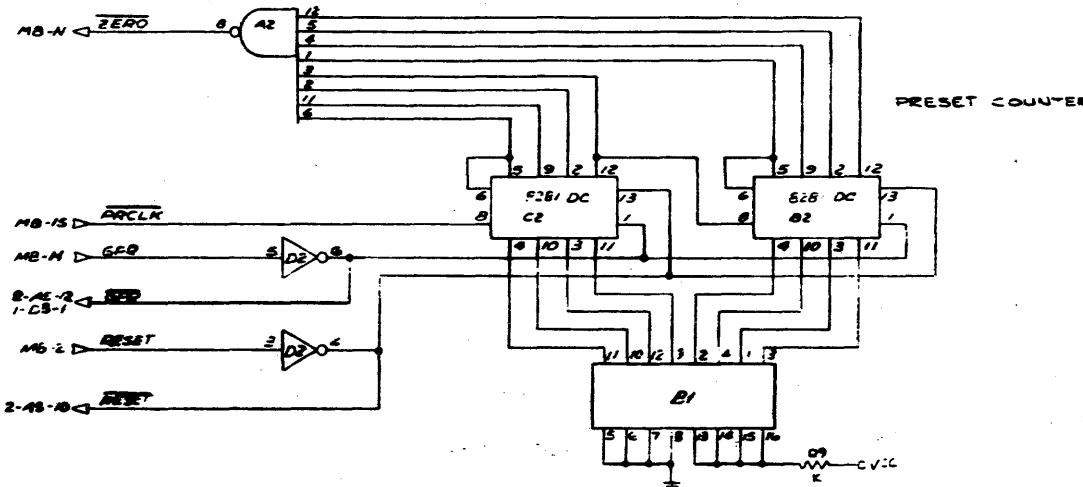


Figure A6. (Sheet 2 of 3)



B1 JUMPER WIRING (PRESET COUNTER)

B1-1	TO	B1-16	(VCC)
-2		-15	(VCC)
-3		-6	(GND)
-4		-6	(GND)
-9		-8	(GND)
-10		-7	(GND)
-11		-6	(GND)
-12		-5	(GND)

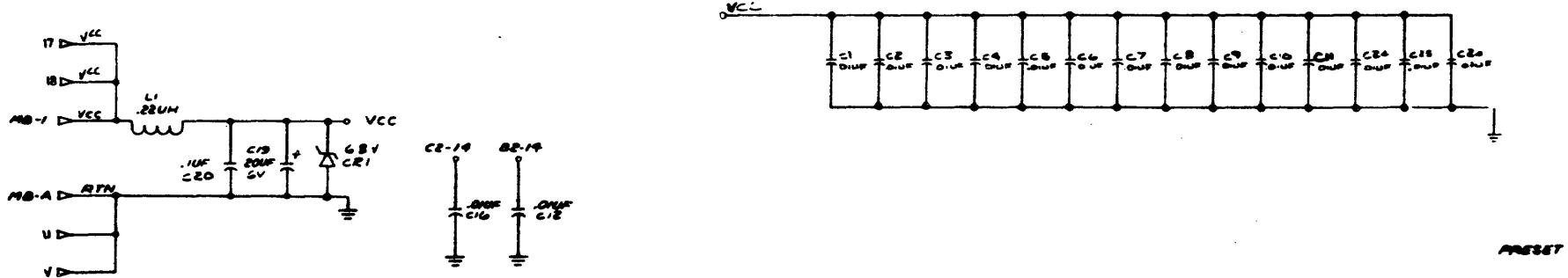


Figure A6. Sync Card Schematic Dwg. No. 1640943 (Sheet 3 of 3) (M-200)

A10

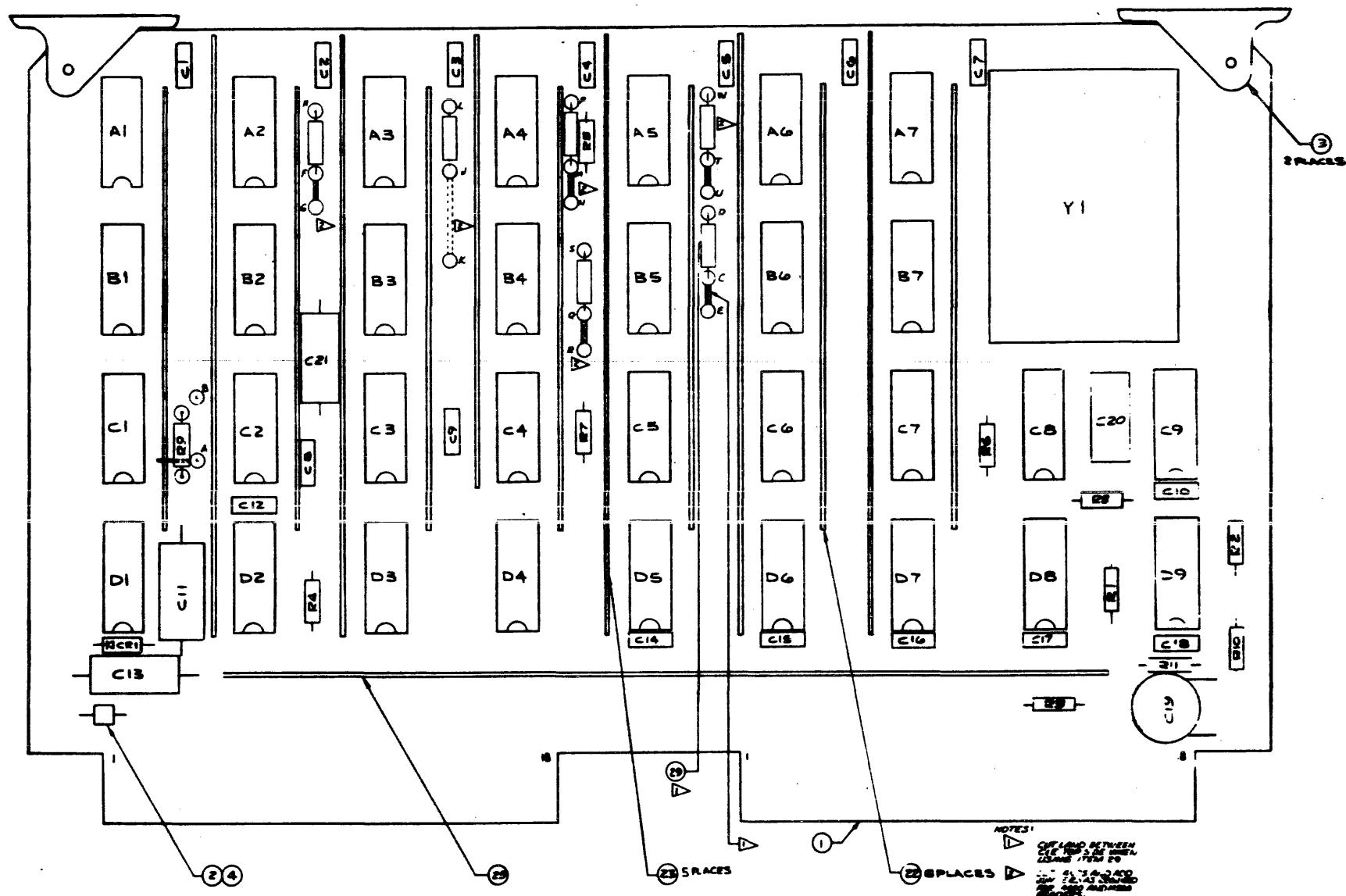


Figure A8. Assembly Diagram, Clock Card
(Dwg. No. 1040765)

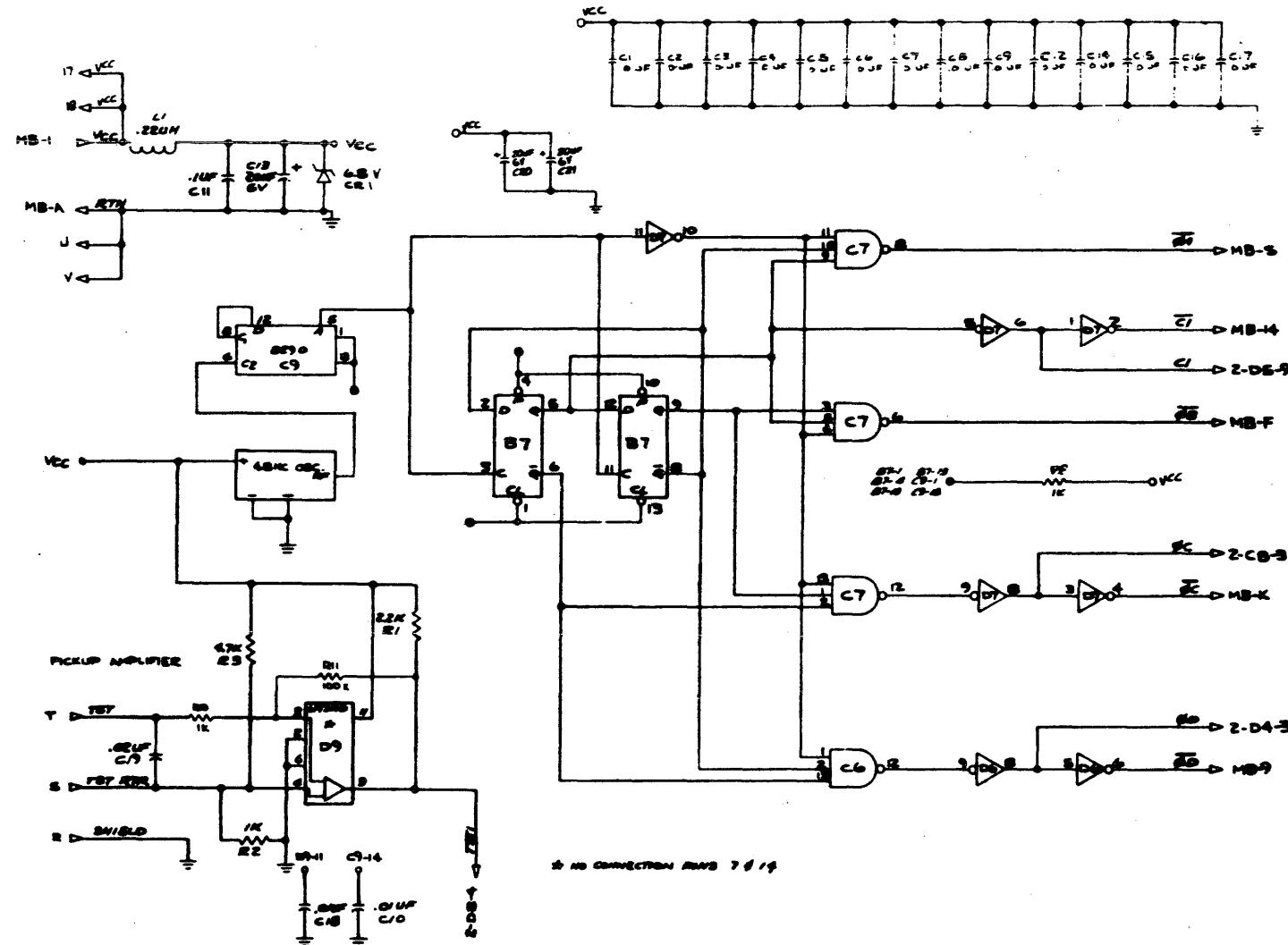


Figure A8. Clock Card Schematic (Sheet 1 of 3)
Dwg. No. 1040800C

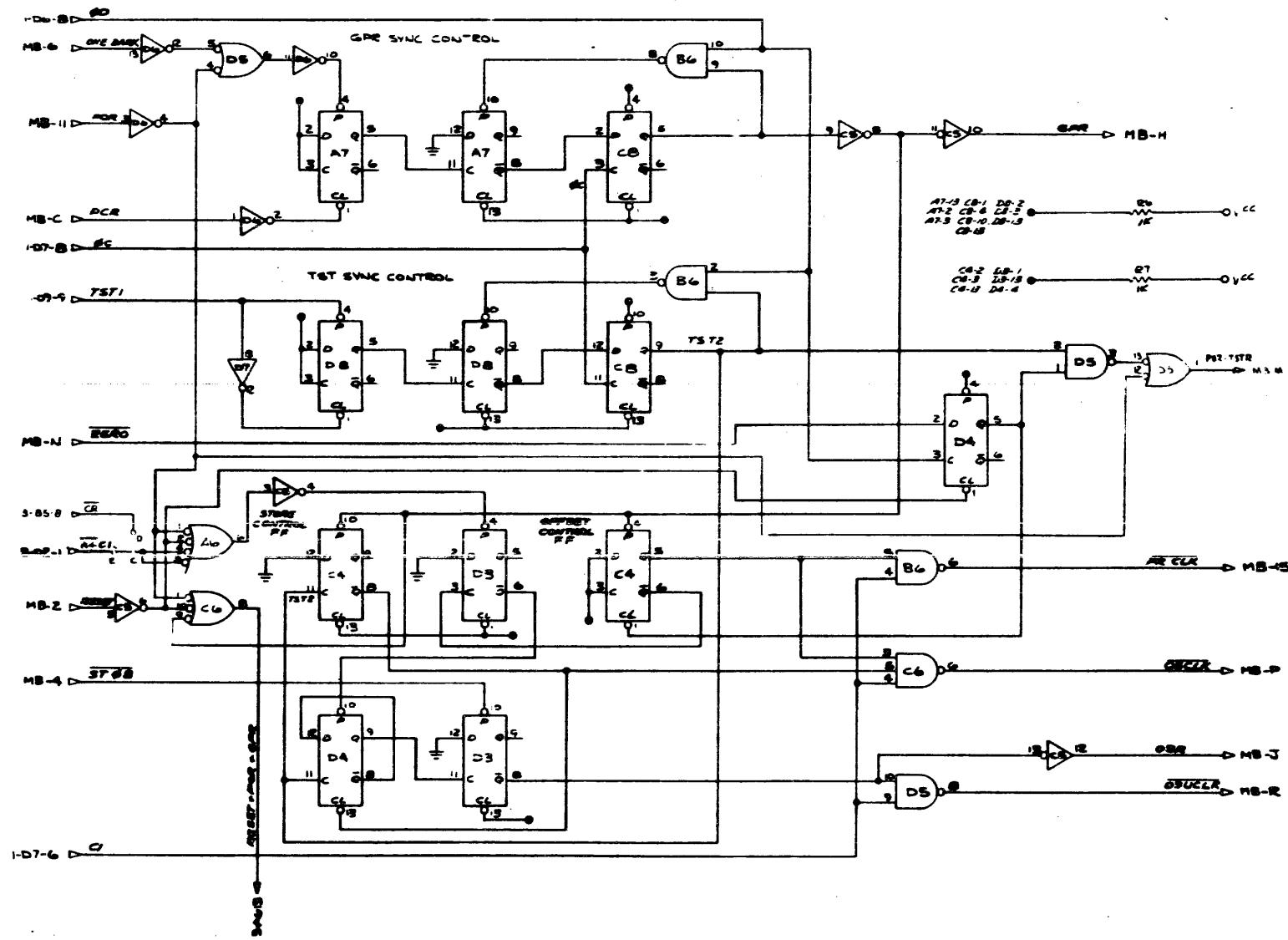
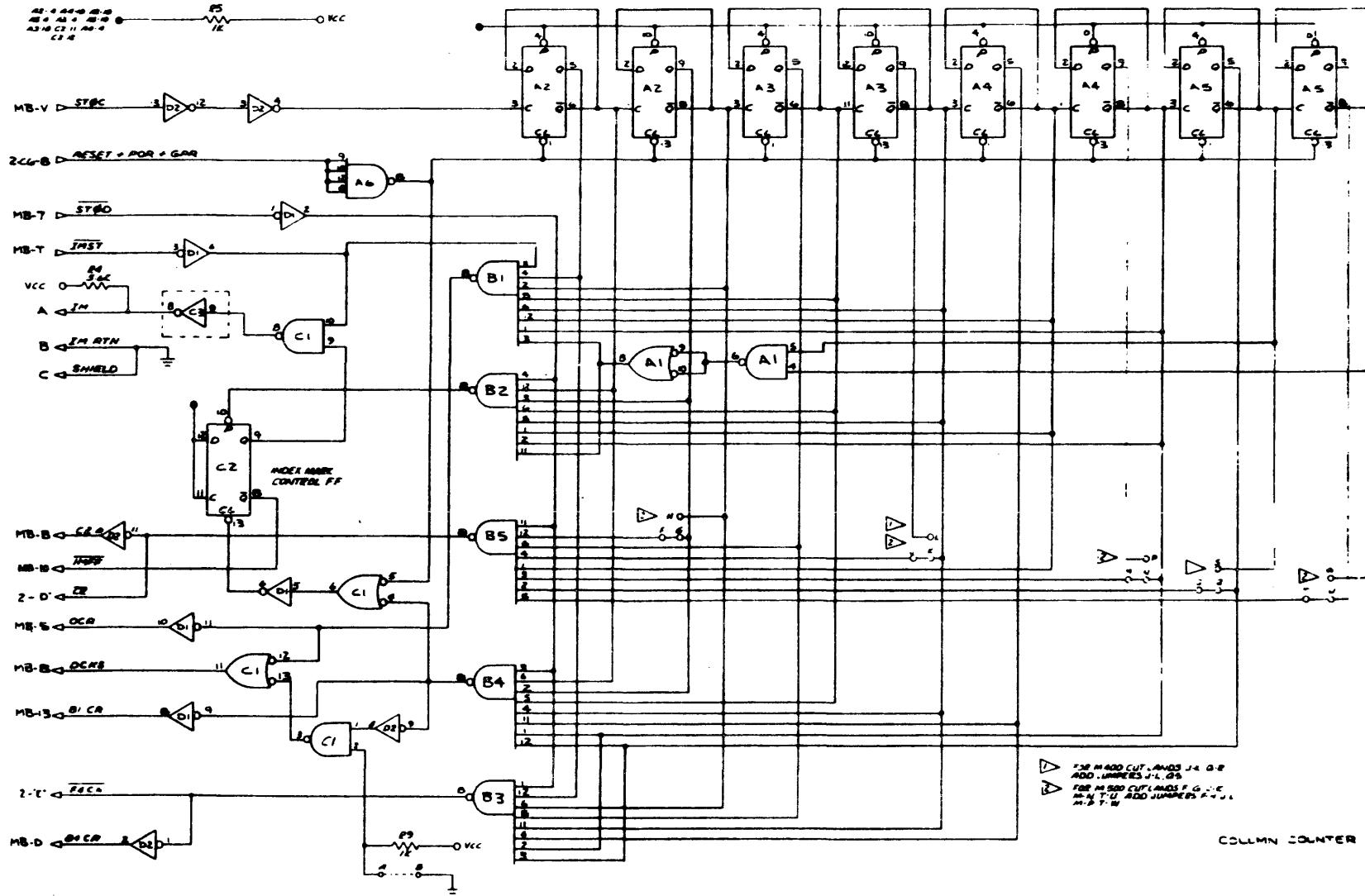


Figure A8. (Sheet 2 of 3)



A14

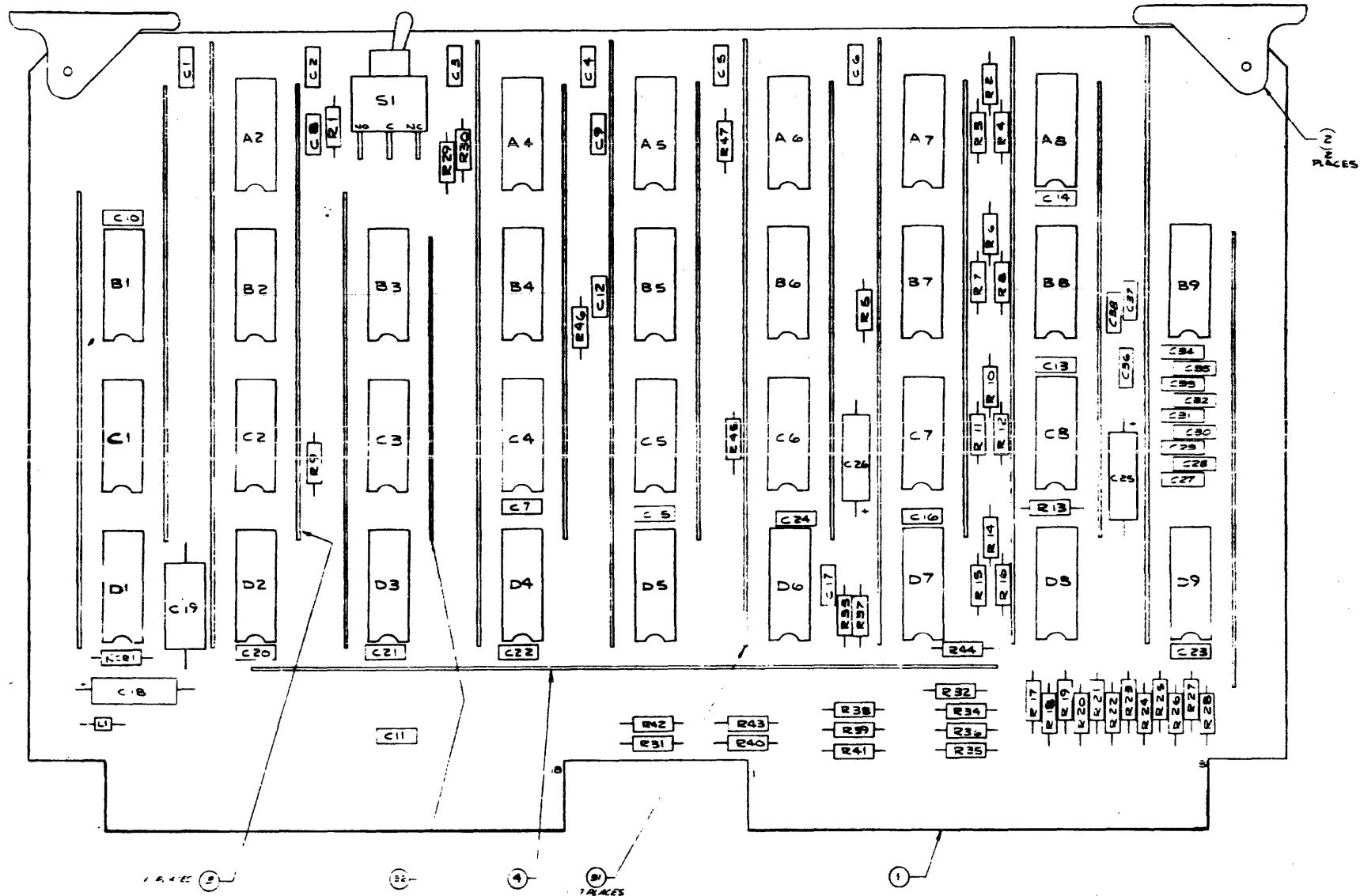


Figure A9. Control Card Assembly
Dwg. No. 1040619

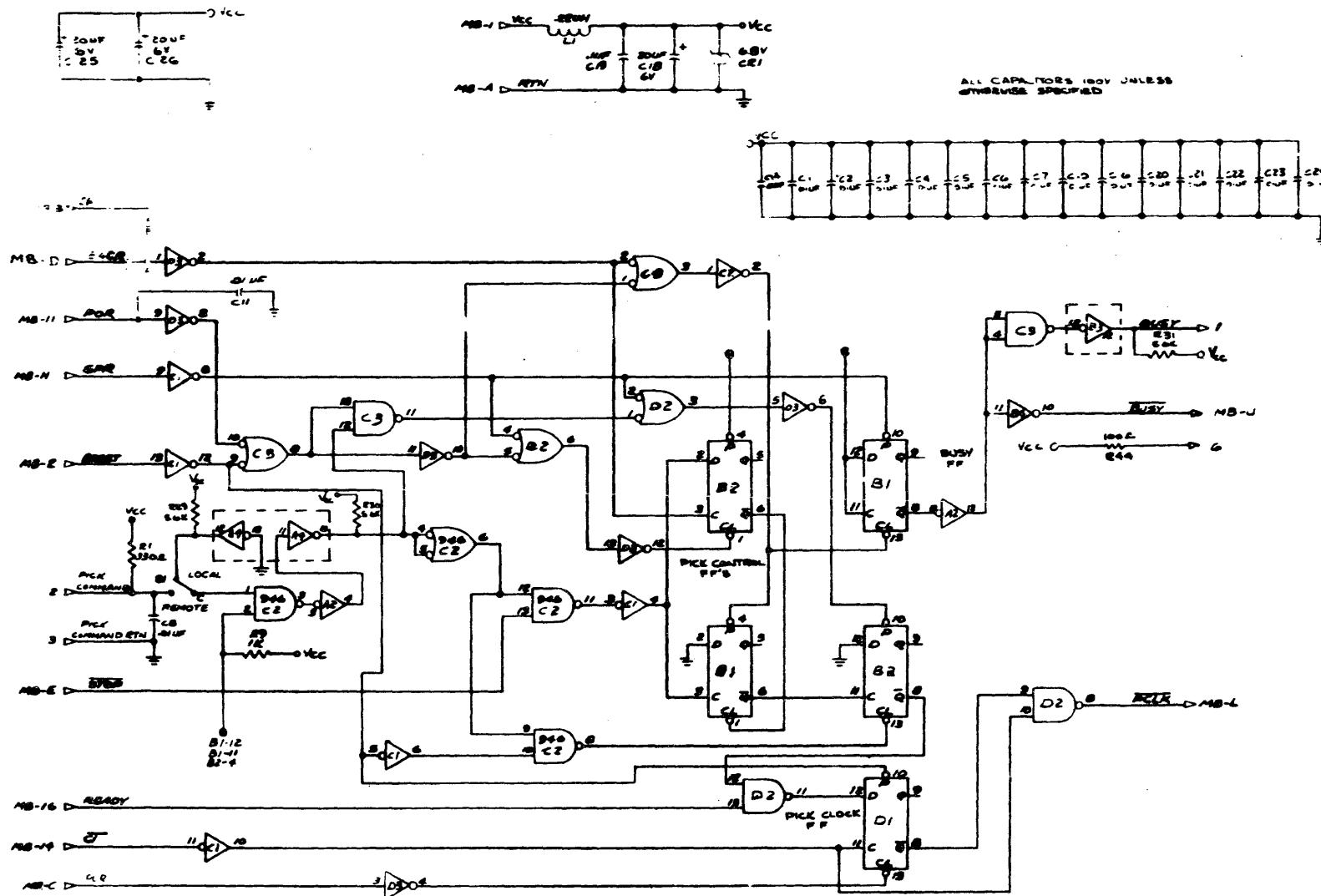


Figure A10. Control Card Schematic (Sheet 1 of 2)
Dwg. No. 1040650D

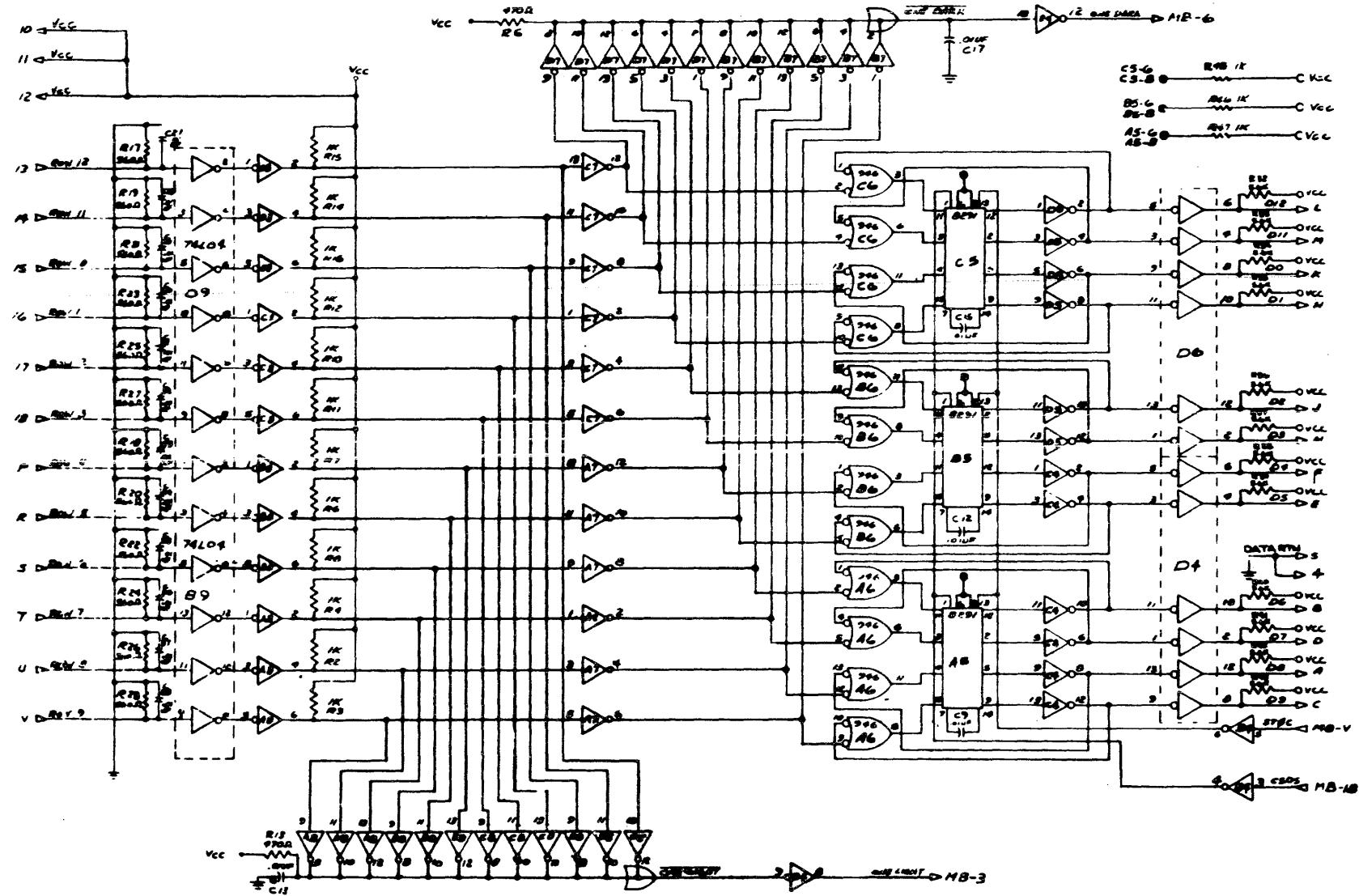
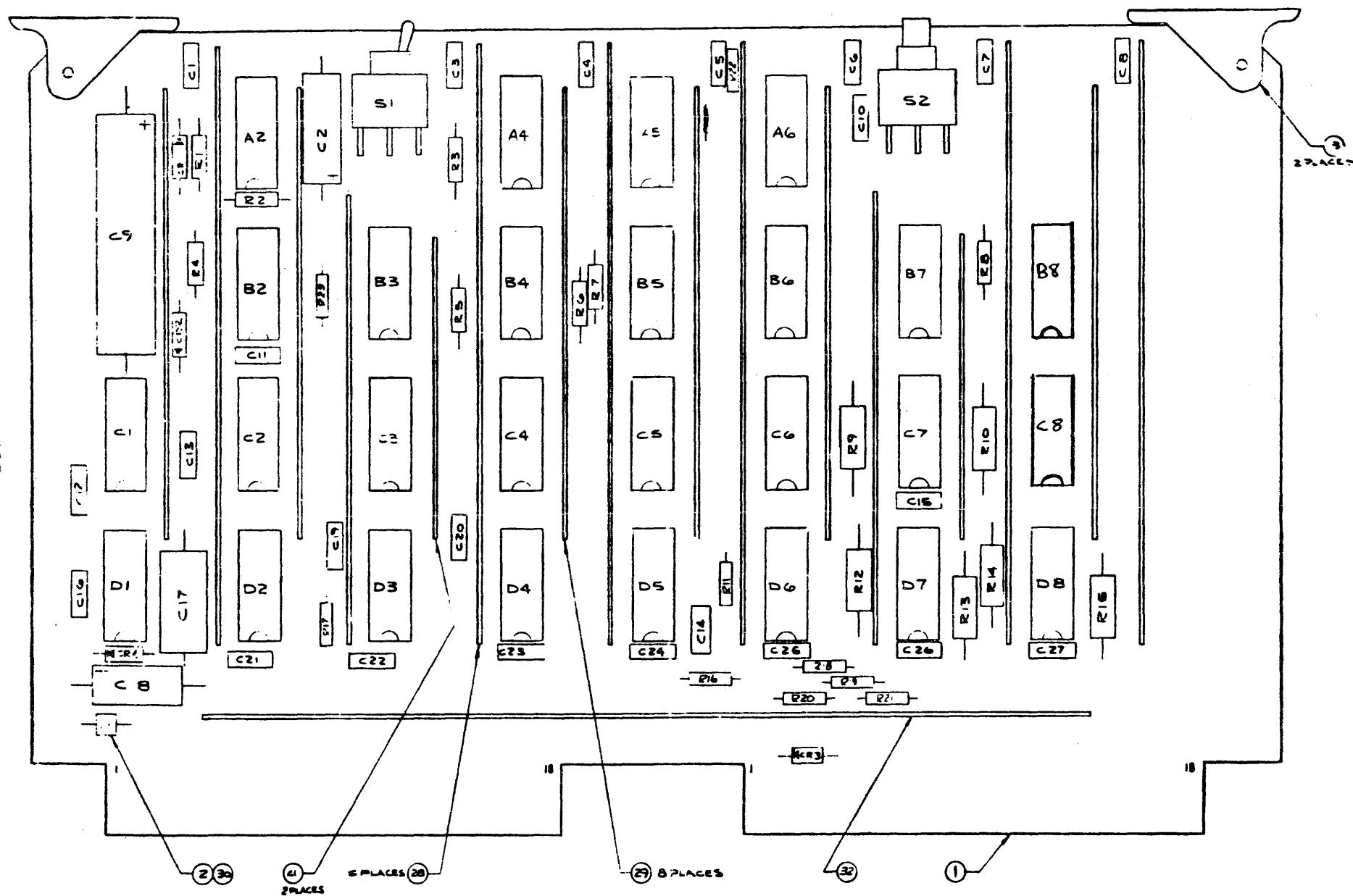
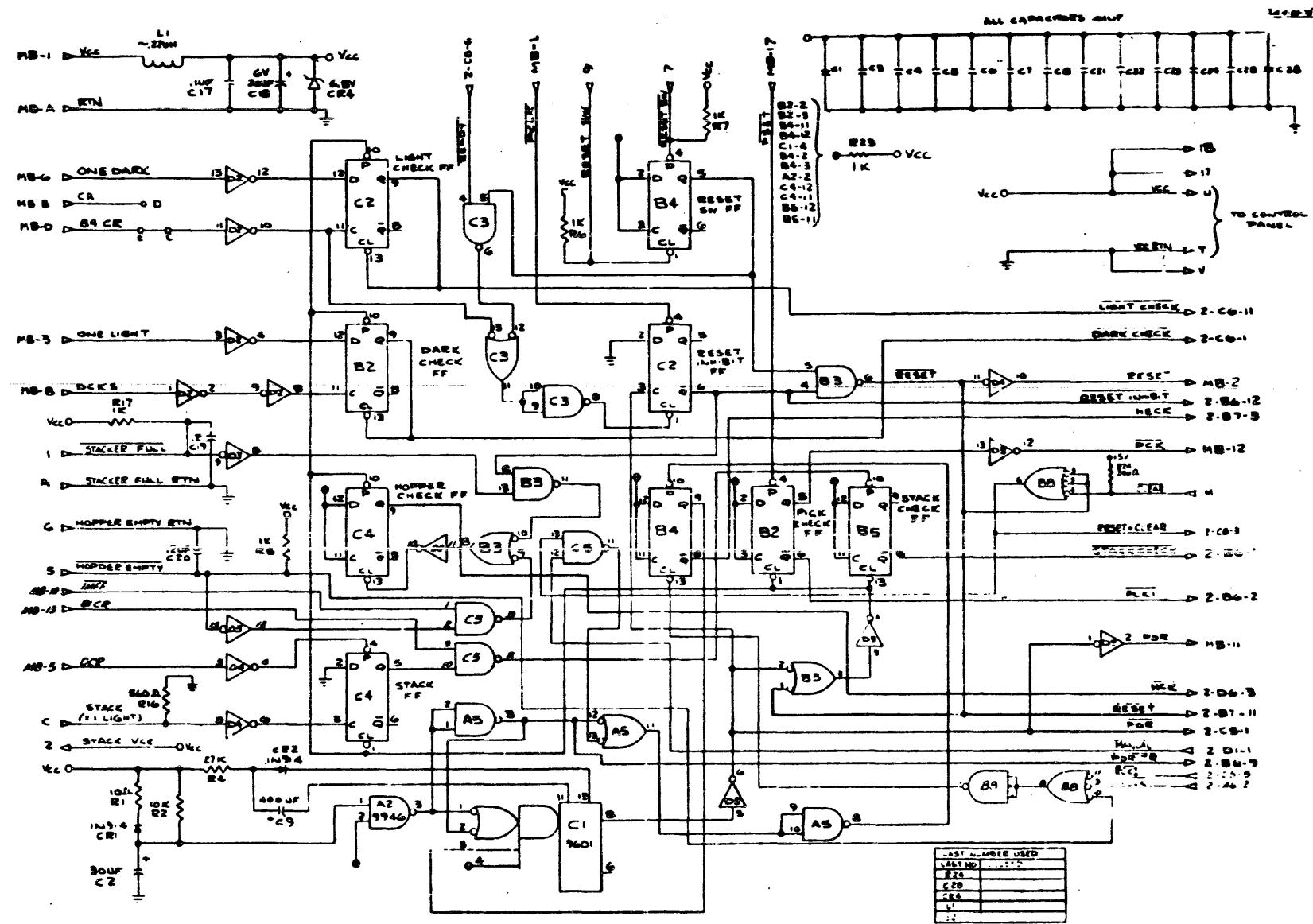


Figure A10. (Sheet 2 of 2)



**Figure A11. Error Card Assembly
(Dwg. No. 1040610)**



H12
Figure A8. Schematic Diagram, Error Card (sheet 1 of 2)
(Dwg. No. 1041908)

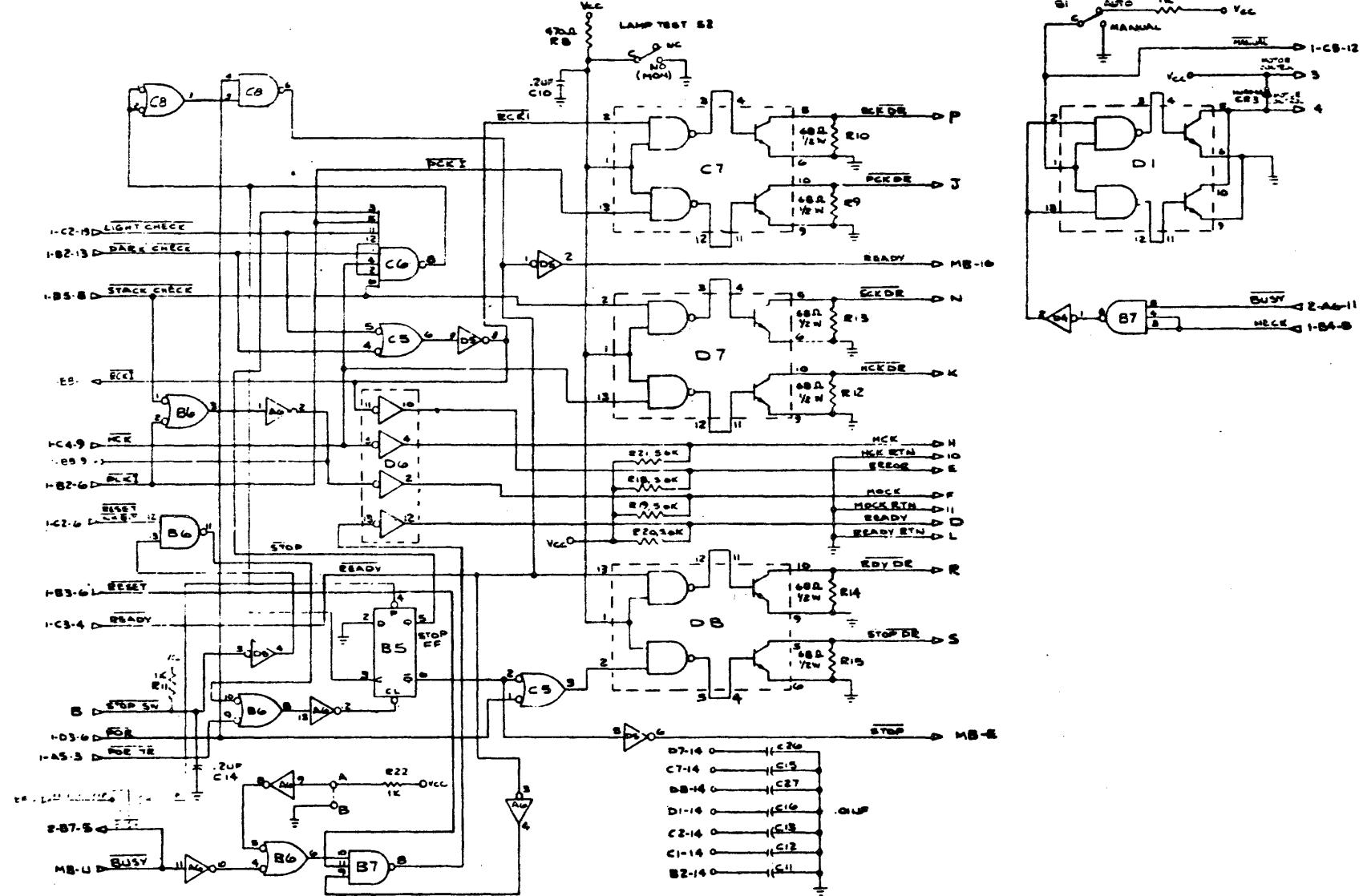


Figure A8. Schematic Diagram, Error Card (sheet 2 of 2)

SIGNAL MNEMONICS AND ABBREVIATIONS

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
Vcc	+5 volts	MB-1	5 volt power supply (Mother Board)
RTN	+5 volt return	MB-A	5 volt power supply (Mother Board)
TST	Timing Strobe	J3-T	Reluctance Pickup
TST RTN	Timing Strobe Return	J3-S	Reluctance Pickup
SHIELD	Shield for Timing Strobe	J3-R	Reluctance Pickup
TST1	Timing Strobe One	D9-9	Clock Card
φA	Clock Phase A	MB-S	Clock Card
C1	Basic Clock	MB-14	Clock Card
φB	Clock Phase B	MB-F	Clock Card
φC	Clock Phase C	MB-K	Clock Card
φD	Clock Phase D	MB-9	Clock Card
ONE DARK	Read Station Any Dark	MB-6	Control Card
POR	Power On Reset	MB-11	Error Card
PCR	Pick Control Reset	MB-C	Sync Card
ZERO	Preset Decode	MB-N	Sync Card
RESET	Gated Reset Switch	MB-2	Sync Card
ST _φ B	Column Strobe Phase B	MB-4	Sync Card
GPR	Good Pick Reset	MB-H	Clock Card
TST2	Timing Strobe Two	C8-9	Clock Card
TSTR	Timing Strobe Reset	MB-N	Clock Card
PRCLK	Preset Clock	MB-15	Clock Card
OSCLK	Offset Clock	MB-P	Clock Card
OSR	Offset Reset	MB-J	Clock Card
OSUCLK	Offset Up-Clock	MB-R	Clock Card
ST _φ C	Column Strobe Phase C	MB-V	Sync Card
ST _φ D	Column Strobe Phase D	MB-7	Sync Card
IMST	Index Mark Strobes	MB-T	Sync Card
IM	Index Marks	J3-A	Clock Card
IM RTN	Return for Index Marks	J3-B	Clock Card
SHIELD	Shield for Index Marks	J3-C	Clock Card
CR	Column Reset	MB-B	Clock Card
OCR	Zero Column Reset	MB-5	Clock Card

SIGNAL MNEMONICS AND ABBREVIATIONS
(Continued)

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
DCKS	Dark Check Strobes	MB-8	Clock Card
81CR	81st Column Reset	MB-13	Clock Card
84CR	84th Column Reset	MB-D	Clock Card
PICK COMMAND	Pick Command Input	J8-2	Control Card
PICK COMMAND RTN	Pick Command Input Return	J8-3	Control Card
STOP	Stop	MB-E	Error Card
READY	Ready	MB-16	Error Card
BUSY	Busy Output	J8-1	Control Card
PCLK	Pick Clock	MB-L	Control Card
Vcc	+5V to Read Sensor Array	J8-12	Control Card
Row 12	Read Sensor Input Row 12	J8-13	Control Card
Row 11	Read Sensor Input Row 11	J8-14	Control Card
Row 0	Read Sensor Input Row 0	J8-15	Control Card
Row 1	Read Sensor Input Row 1	J8-16	Control Card
Row 2	Read Sensor Input Row 2	J8-17	Control Card
Row 3	Read Sensor Input Row 3	J8-18	Control Card
Row 4	Read Sensor Input Row 4	J8-P	Control Card
Row 5	Read Sensor Input Row 5	J8-R	Control Card
Row 6	Read Sensor Input Row 6	J8-S	Control Card
Row 7	Read Sensor Input Row 7	J8-T	Control Card
Row 8	Read Sensor Input Row 8	J8-U	Control Card
Row 9	Read Sensor Input Row 9	J8-V	Control Card
ONE LIGHT	Read Station Any Light	MB-3	Control Card
D12	Data Row 12 Output	J8-L	Control Card
D11	Data Row 11 Output	J8-M	Control Card
D0	Data Row 0 Output	J8-K	Control Card
D1	Data Row 1 Output	J8-H	Control Card
D2	Data Row 2 Output	J8-J	Control Card
D3	Data Row 3 Output	J8-N	Control Card
D4	Data Row 4 Output	J8-F	Control Card
D5	Data Row 5 Output	J8-E	Control Card
RTN	Data Drivers Return	J8-5	Control Card
D6	Data Row 6 Output	J8-B	Control Card

SIGNAL MNEMONICS AND ABBREVIATIONS
(Continued)

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
D7	Data Row 7 Output	J8-D	Control Card
D8	Data Row 8 Output	J8-A	Control Card
D9	Data Row 9 Output	J8-C	Control Card
CSDS	Column Storage Data Strobe	MB-18	Sync Card
HOPPER FULL	Hopper Full Switch	J4-1	Error Card
HOPPER FULL RTN	Hopper Full Switch Return	J4-A	Error Card
HOPPER EMPTY RTN	Hopper Empty Switch Return	J4-6	Error Card
HOPPER EMPTY	Hopper Empty Switch	J4-5	Error Card
STACK	Stack Sensor Input	J4-C	Error Card
STACK Vcc	Stack Sensor +5 volts	J4-2	Error Card
RESET SW	Reset Switch Normally Open	J4-9	Error Card
<u>RESET SW</u>	Reset Switch Normally Closed	J4-7	Error Card
PSET	Pick Check Set	MB-17	Sync Card
LIGHT CHECK	Light Check	C2-9	Error Card
DARK CHECK	Dark Check	B2-9	Error Card
HECK	Hopper Empty Check	B4-8	Error Card
PCK	Pick Check	B2-5	Error Card
STACK CHECK	Output Stacker Check	B5-8	Error Card
PCKI	Pick Check Indicator	B2-2	Error Card
HCK	Input or Output Hopper Check	C4-9	Error Card
SHUTDOWN STATUS	Mode Switch Input	S1-C	Error Card
POR TR	Power on Reset Trigger	A5-12	Error Card
STOP SW	Stop Switch Input	J4-B	Error Card
RCK DR	Read Check Lamp Driver	J4-P	Error Card
PCK DR	Pick Check Lamp Driver	J4-P	Error Card
SCK DR	Stack Check Lamp Driver	J4-N	Error Card
HCK DR	Hopper Check Lamp Driver	J4-K	Error Card
HCK	Hopper Check Output	J4-H	Error Card
HCK RTN	Hopper Check Output Return	J4-10	Error Card
ERROR	Error Output	J4-E	Error Card
ERROR RTN	Error Output Return	J4-M	Error Card
MOCK	Motion Check Output	J4-F	Error Card

SIGNAL MNEMONICS AND ABBREVIATIONS
(Continued)

MNEMONIC	DESCRIPTION	LOCATION	ORIGINATING SOURCE
MOCK RTN	Motion Check Output Return	J4-11	Error Card
READY	Ready Output	J4-D	Error Card
READY RTN	Ready Output Return	J4-L	Error Card
RDY DR	Ready Lamp Driver	J4-R	Error Card
STOP DR	Stop Lamp Driver	J4-S	Error Card
PICK	Pick Driver Output	J5-A	Sync Card
PICK RTN	Pick Driver Output Return	J5-B	Sync Card
SHIELD	Shield for PICK	J5-C	Sync Card
BUSY	Busy Signal	MB-U	Control Card